Design Theory for High-Order Incremental Converters

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Outline (Highlights)

- Digital measurement of DC signals
- Incremental (integrating) $\Delta\Sigma$ converter basics
- Analysis of higher-order architectures
- Digital filter design techniques
Digital Measurement of DC Signals

Applications

- Sensors (seismic, pressure, temperature...)
- Process monitoring and control
- Instrumentation, digital voltmeter

Requirements

- Low offset- and gain-error
- Good linearity, high accuracy (up to 18-20-24 bits)
- Low power consumption
- Low speed
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A/D Converters for DC Measurement

Classical Nyquist-rate Converters
- Dual-slope, V-to-freq converters
  - Sensitivity to noise and mismatches

ΔΣ converters
- Producing offset and tones
- Non-multiplex

Incremental converter
+ Great tolerance
+ No tones and offset
Based on a $\Delta \Sigma$ structure

Transient operation, simpler digital filter

No-latency, one-shot, one-cycle, no-missing-code, charge-balancing $\Delta \Sigma$ converter
Due to the higher loop-gain

- Faster operation can be achieved
- Scaling coefficients $b$ and $c_i$ are required
First integrator’s output:

\[ V_{i1}[1] = b(V_{in}[0] - d_0 V_{ref}) \]
\[ V_{i1}[n] = b \sum_{k=0}^{n-1} (V_{in}[k] - d_k V_{ref}) \]
Second integrator’s output:

\[ V_{i2}[n] = c_1 \sum_{l=0}^{n-1} V_{i1}[l] = c_1 b \sum_{l=0}^{n-1} \sum_{k=0}^{l-1} (V_{in}[k] - d_k V_{ref}) \]
Operation Principle III.

Second integrator’s output:

\[ V_{i2}[n] = c_1 b \sum_{l=0}^{n-1} \sum_{k=0}^{l-1} (V_{\text{in}}[k] - d_k V_{\text{ref}}) \]

If \( V_{i2}[n] \) is bounded by \( \pm V_{\text{ref}} \) (i.e. stable), then (assuming DC input):

\[
- \frac{2!}{n - 1) n} \frac{1}{c_1 b} V_{\text{ref}} < V_{\text{in}} - \frac{2!}{(n - 1) n} V_{\text{ref}} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k < \\
+ \frac{2!}{n - 1) n} \frac{1}{c_1 b} V_{\text{ref}}
\]
Output Calculation

\[
\frac{\hat{V}_{\text{in}}}{V_{\text{ref}}} = \frac{2!}{(n-1)n} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k
\]

Properties:

+ The output is independent of the scaling coefficients \( b \) and \( c_i \)
+ The quantization error is available in analog form
  \[
  (V_{i_2}[n] = -2V_{\text{ref}} e_q)
  \]
+ Does not suppress periodic noise disturbances
The LSB value is

\[ V_{\text{LSB}} = \frac{2 \cdot 2!}{(n - 1)n c_1 b} V_{\text{ref}}, \]

thus, the resolution becomes

\[ n_{\text{bit}} = \log_2 \left( \frac{2V_{\text{ref}}}{V_{\text{LSB}}} \right) = \log_2 \left( c_1 b \frac{(n - 1)n}{2!} \right) \approx 2 \log_2 (n) + \log_2 (c_1 b) - 1 \]

Properties:

+ \( n_{\text{bit}} \sim 2 \log_2 (n) \)

- \( n_{\text{bit}} \) depends on the scaling coefficients
Effect of the Scaling Coefficients

- Resolution increases rapidly with $n$
- $b < 1$, $c_i < 1$, both are inversely proportional to $n$
- For 16-bit resolution $n = 363$ is required if $b = 1$, $c_i = 1$
- With proper scaling, this goes up ($n \geq 537$)
- One can find the lowest $n$ easily by a couple of iterative simulations
Recalling the output-calculation:

\[
\frac{\hat{V}_{\text{in}}}{V_{\text{ref}}} = \frac{2!}{(n-1)n} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k
\]

- Direct Realization: Cascade-of-Integrators (CoI) filter
- First-order integration cancels periodic disturbances if operation time matches \( 1/f_l \)
  - Higher-order integration does not cancel periodic disturbances
Use CIC (sinc) filter instead of CoI:

Properties:

+ $L^{th}$-order suppression of line frequency disturbances
- Requires more cycles to fulfill a given resolution requirement
<table>
<thead>
<tr>
<th>Order of Modulator</th>
<th>Type of Digital Filter</th>
<th>Resolution (Accuracy)</th>
<th>Total Number of Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 integrator (counter)</td>
<td>16</td>
<td>65536</td>
</tr>
<tr>
<td>2</td>
<td>2 integrators</td>
<td>16</td>
<td>537</td>
</tr>
<tr>
<td>2</td>
<td>third-order sinc</td>
<td>16</td>
<td>576</td>
</tr>
</tbody>
</table>
Conclusion

- Digital measurement of DC signals
- Incremental (integrating) ΔΣ converter basics
  - First-order converter
- Analysis of higher-order architectures
  - Structure
  - Operation
- Digital filter design techniques
  - Cascade-of-Integrators (CoI) filter
  - CIC (sinc) filters
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First-Order Converter II. [robert84]

- $V_{in} = 0.075V_{ref}$
- $D_{out} = 5$
- $n_{bit} = 6$
- $n = 64$
- $D_{norm} = 5/64 = 0.0781$
Improved Line Frequency Suppression

![Graph showing improved line frequency suppression with deviation from the notch frequency [%] on the x-axis and attenuation of the filter [dB] on the y-axis. The graph compares third-order and fourth-order filters.]

Incremental Converters (WISP’2003) – p.18
Improved Line Frequency Suppression

- Required if line and/or oscillator frequency drifts
- Can be realized by the rotated sinc-filter

Incremental Converters (WISP’2003) – p.18