Design Theory for High-Order Incremental Converters

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Outline (Highlights)

- Digital measurement of DC signals
- Incremental (integrating) $\Delta\Sigma$ converter basics
- Analysis of higher-order architectures
- Digital filter design techniques

Digital Measurement of DC Signals

- **Applications**
  - **Sensors (seismic, pressure, temperature. . .)**
  - **Process monitoring and control**
  - **Instrumentation, digital voltmeter**

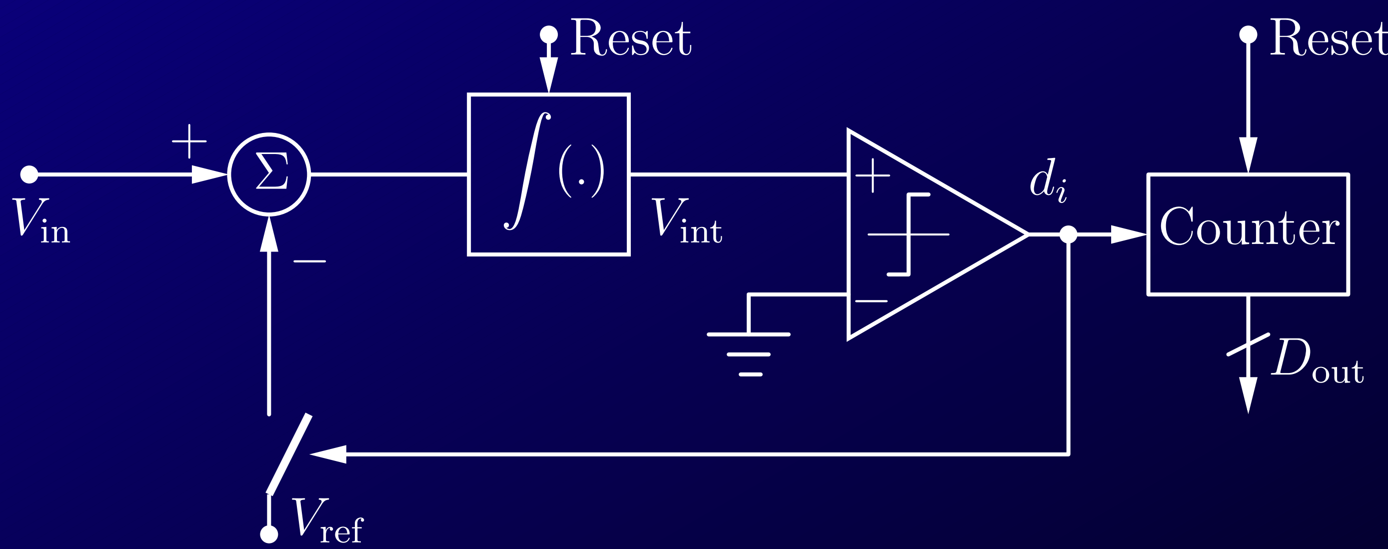
Digital Measurement of DC Signals

- Applications
  - Sensors (seismic, pressure, temperature. . .)
  - Process monitoring and control
  - Instrumentation, digital voltmeter
- Requirements
  - Low offset- and gain-error
  - Good linearity, high accuracy (up to 18-20-24 bits)
  - Low power consumption
  - Low speed

A/D Converters for DC Measurement

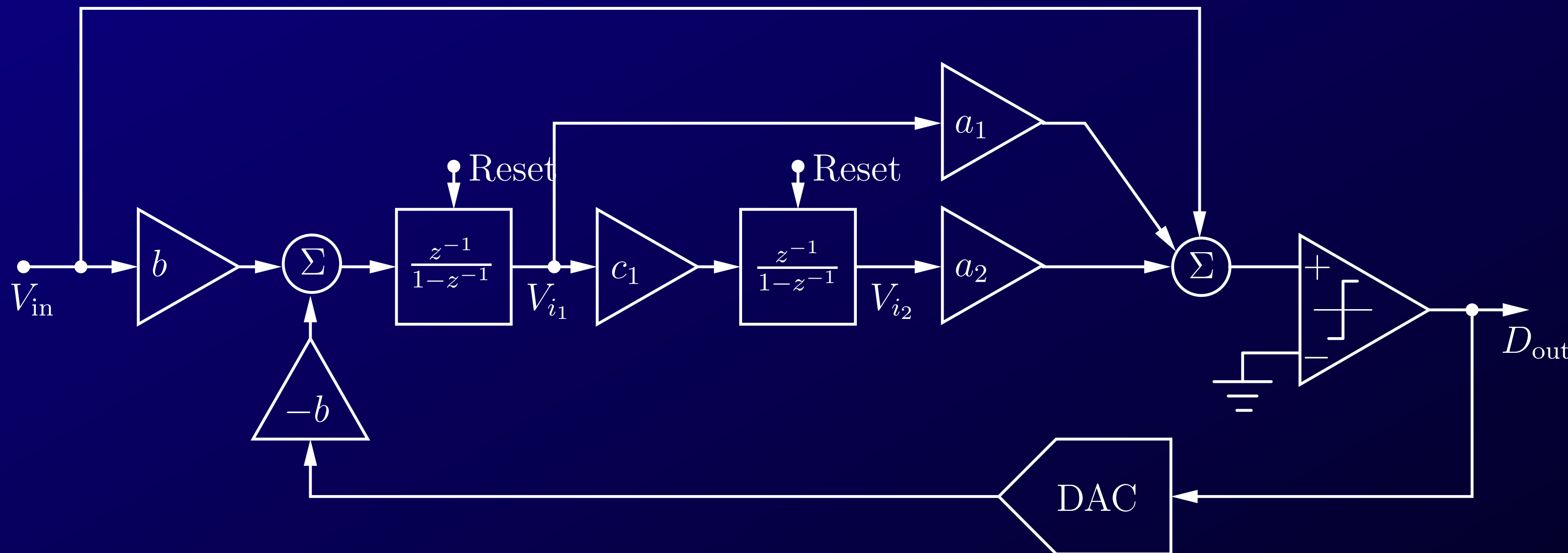
- Classical Nyquist-rate Converters
  - Dual-slope, V-to-freq converters
  - – Sensitivity to noise and mismatches
- $\Delta\Sigma$ converters
  - – Producing offset and tones
  - – Non-multiplex
- Incremental converter
  - + Great tolerance
  - + No tones and offset

First-Order Converter [robert84]



- **Based on a $\Delta\Sigma$ structure**
- **Transient operation, simpler digital filter**
- **No-latency, one-shot, one-cycle, no-missing-code, charge-balancing $\Delta\Sigma$ converter**

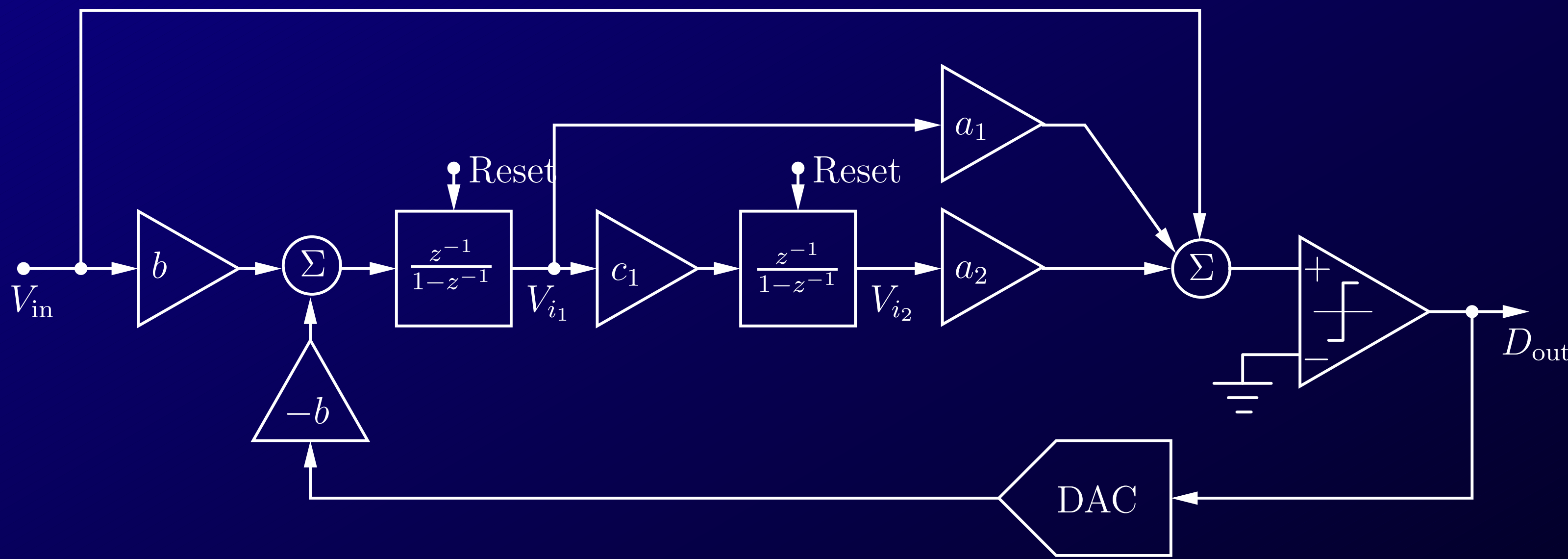
Higher-Order Incremental Converters



Due to the higher loop-gain

- $+$ **Faster operation can be achieved**
- $-$ **Scaling coefficients b and c_i are required**

Operation Principle I.

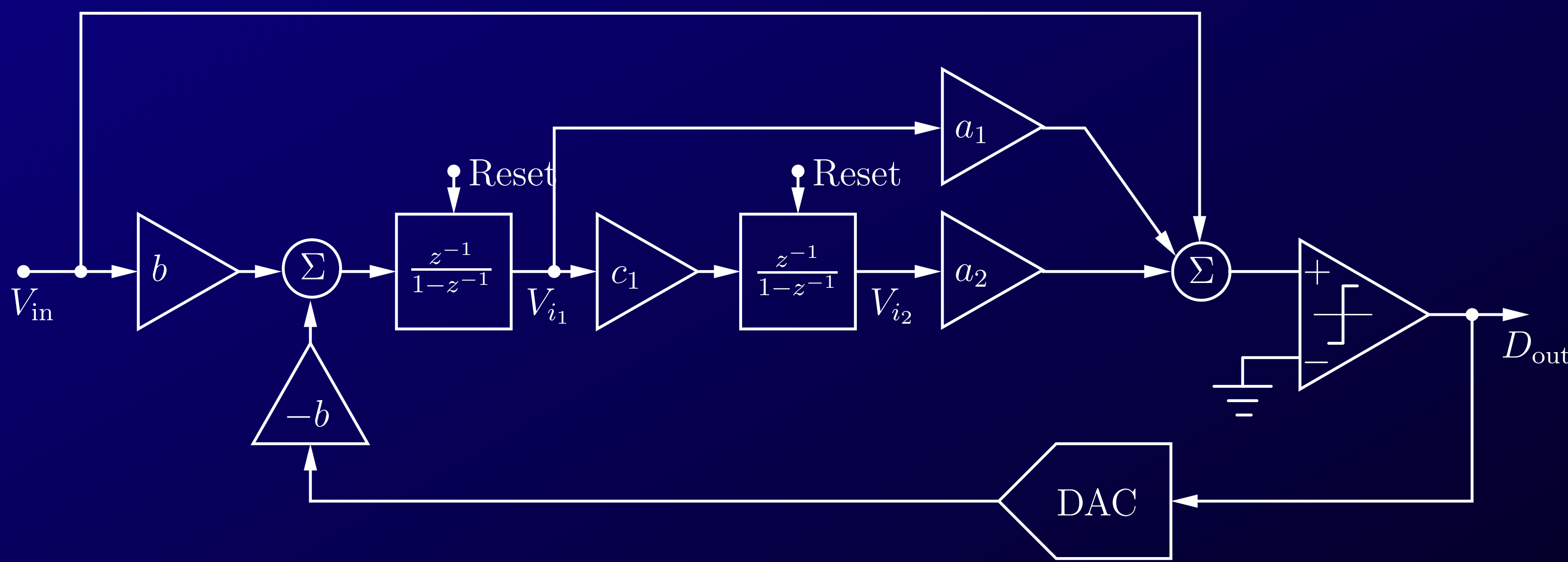


First integrator's output:

$$V_{i_1}[1] = b(V_{\mathrm{in}}[0] - d_0 V_{\mathrm{ref}})$$

$$V_{i_1}[n] = b\sum_{k=0}^{n-1}(V_{\mathrm{in}}[k] - d_k V_{\mathrm{ref}})$$

Operation Principle II.



Second integrator's output:

$$V_{i_2}[n] = c_1 \sum_{l=0}^{n-1} V_{i_1}[l] = c_1 b \sum_{l=0}^{n-1} \sum_{k=0}^{l-1} (V_{\text{in}}[k] - d_k V_{\text{ref}})$$

Operation Principle III.

Second integrator's output:

$$V_{i_2}[n] = c_1 b \sum_{l=0}^{n-1} \sum_{k=0}^{l-1} (V_{\text{in}}[k] - d_k V_{\text{ref}})$$

If $V_{i_2}[n]$ is bounded by $\pm V_{\text{ref}}$ (i.e. stable), then (assuming DC input):

$$-\frac{2!}{(n-1)n}\frac{1}{c_1 b}V_{\text{ref}} < V_{\text{in}} - \frac{2!}{(n-1)n}V_{\text{ref}} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k < + \frac{2!}{(n-1)n}\frac{1}{c_1 b}V_{\text{ref}}$$

Output Calculation

$$\frac{\hat{V}_{\text{in}}}{V_{\text{ref}}} = \frac{2!}{(n-1)n} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k$$

Properties:

+ **The output is independent of the scaling coefficients b and c_i**
+ **The quantization error is available in analog form ($V_{i_2}[n] = -2V_{\text{ref}} e_q$)**
− **Does not suppress periodic noise disturbances**

Resolution

The LSB value is

$$V_{\mathrm{LSB}} = \frac{2 \cdot 2!}{(n-1)n} \frac{1}{c_1 b} V_{\mathrm{ref}},$$

thus, the resolution becomes

$$n_{\mathrm{bit}} = \log_2\left(\frac{2V_{\mathrm{ref}}}{V_{\mathrm{LSB}}}\right) = \log_2\left(c_1 b \frac{(n-1)n}{2!}\right)$$
$$\approx 2\log_2(n) + \log_2(c_1 b) - 1$$

Properties:

$+$ $n_{\mathrm{bit}} \sim 2\log_2(n)$

$-$ n_{bit} **depends on the scaling coefficients**

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Effect of the Scaling Coefficients

- **Resolution increases rapidly with n**
- $b < 1$, $c_i < 1$, **both are inversely proportional to** n
- **For 16-bit resolution** $n = 363$ **is required if** $b = 1$, $c_i = 1$
- **With proper scaling, this goes up (**$n \geq 537$**)**
- **One can find the lowest** n **easily by a couple of iterative simulations**

Digital Filter Design I.

Recalling the output-calculation:

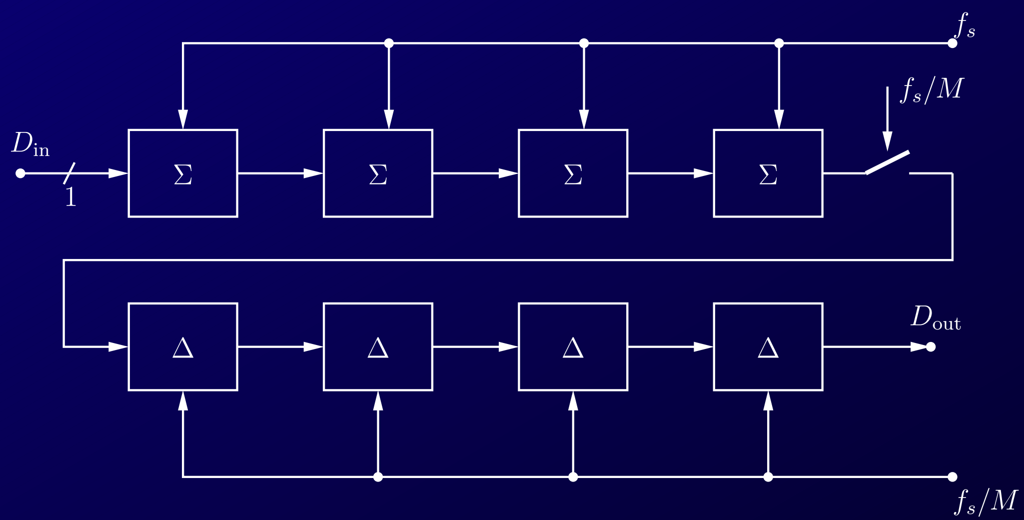
$$\frac{\hat{V}_{\rm in}}{V_{\rm ref}} = \frac{2!}{(n-1)n} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k$$

- **Direct Realization: Cascade-of-Integrators (CoI) filter**
- **First-order integration cancels periodic disturbances if operation time matches $1/f_l$**

– **Higher-order integration does not cancel periodic disturbances**

Digital Filter Design II.

Use CIC (sinc) filter instead of CoI:



Properties:

+ L^{th}-order suppression of line frequency disturbances
– Requires more cycles to fulfill a given resolution requirement

Comparison

Order of Modulator	Type of Digital Filter	Resolution (Accuracy)	Total Number of Cycles
1	1 integrator (counter)	16	65536
2	2 integrators	16	537
2	third-order sinc	16	576

Conclusion

- Digital measurement of DC signals
- Incremental (integrating) $\Delta\Sigma$ converter basics
  - First-order converter
- Analysis of higher-order architectures
  - Structure
  - Operation
- Digital filter design techniques
  - Cascade-of-Integrators (CoI) filter
  - CIC (sinc) filters

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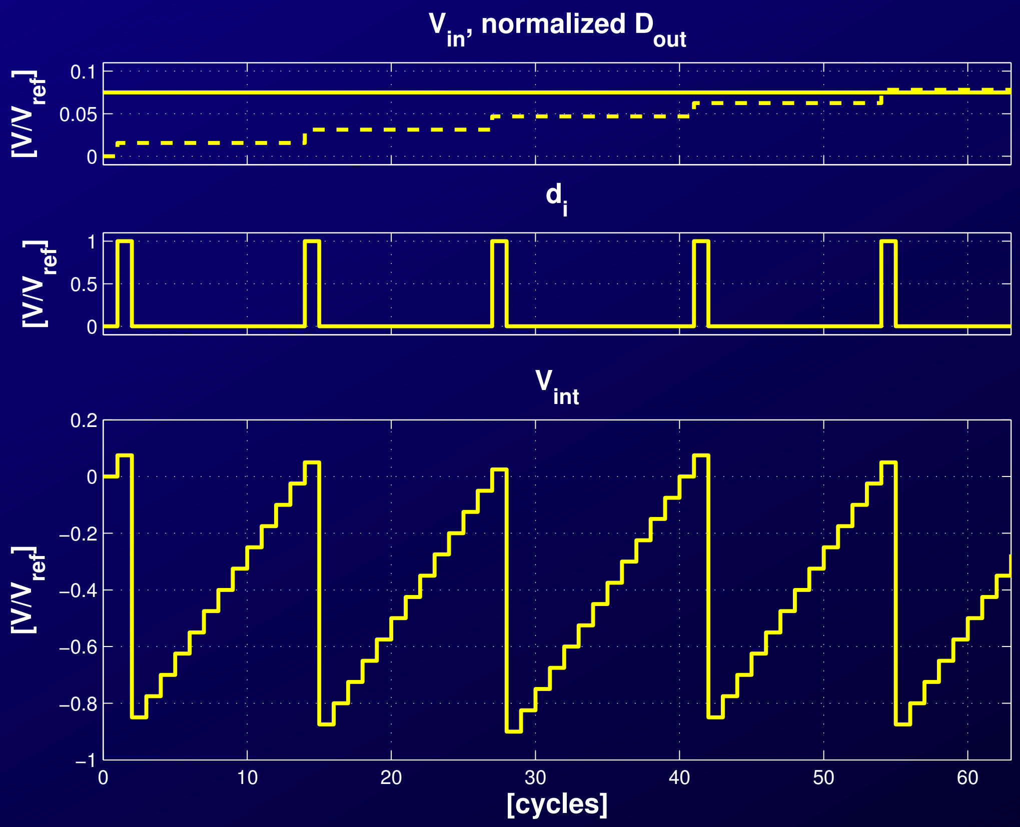
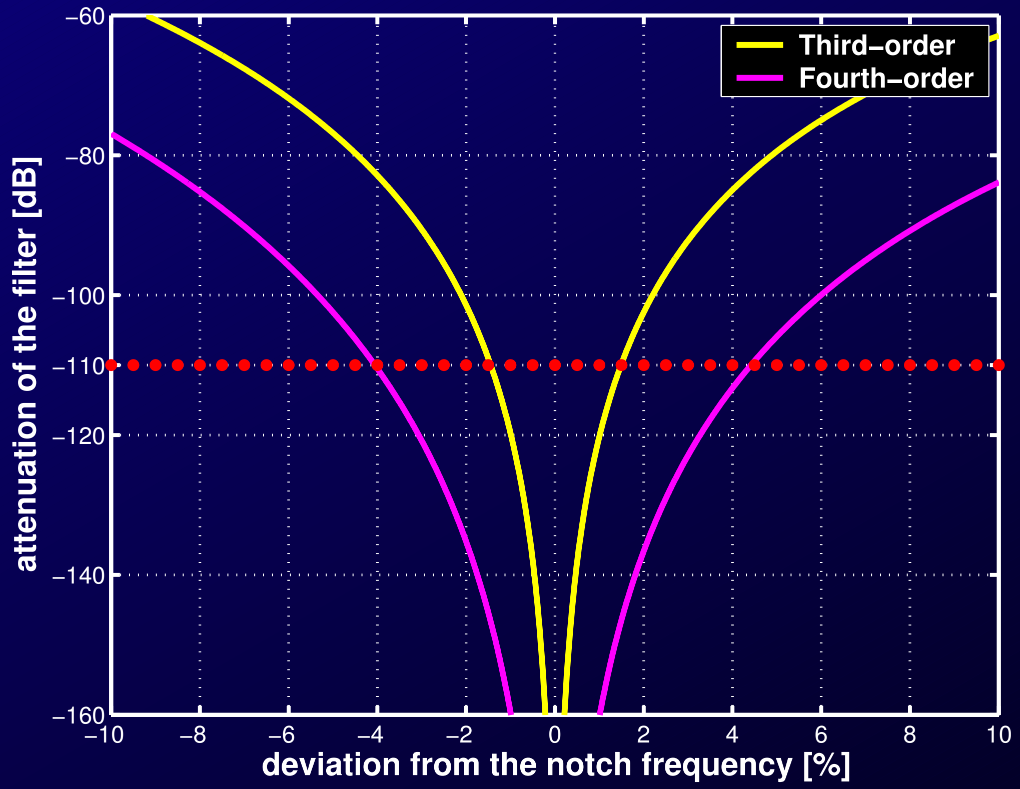
First-Order Converter II. [robert84]



- $V_{\rm in} = 0.075 V_{\rm ref}$
- $D_{\rm out} = 5$
- $n_{\rm bit} = 6$
- $n = 64$
- $D_{\rm norm} = 5/64 = 0.0781$

Improved Line Frequency Suppression



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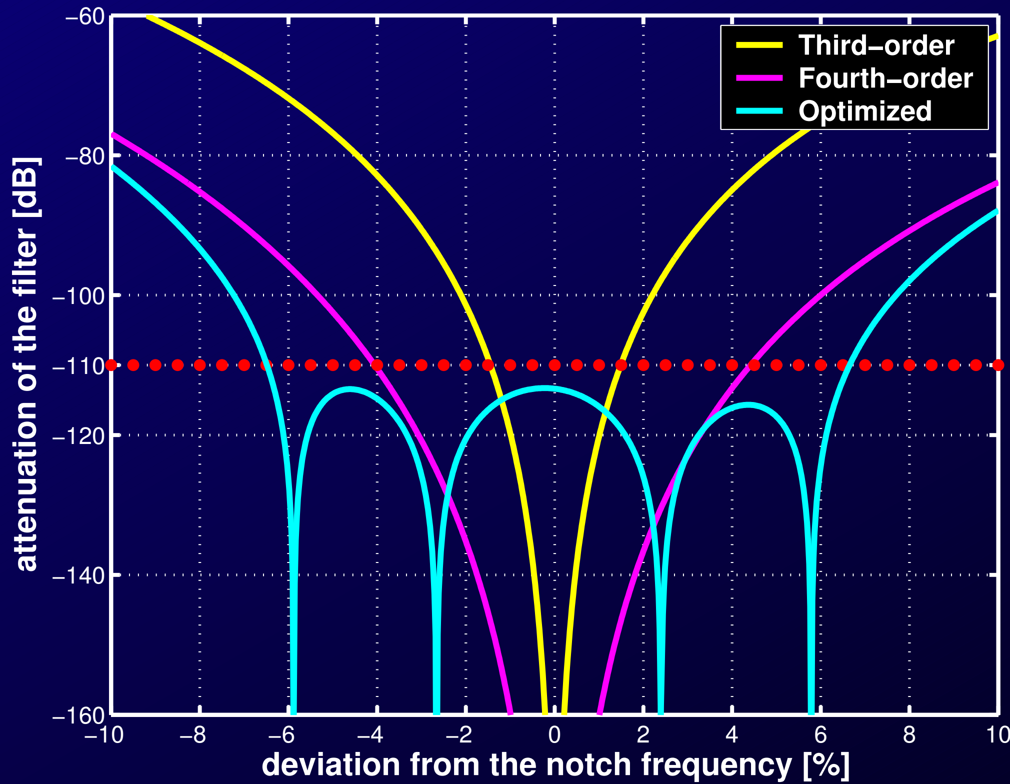

- **Required if line and/or oscillator frequency drifts**
- **Can be realized by the rotated sinc-filter**