Design Theory for High-Order Incremental Converters

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***Abstract** – A/D converters used in instrumentation and measurements often require high* **absolute** *accuracy, including high linearity and negligible DC offset. The incremental (or integrating) converter provides a solution for such measurement applications, as it has all the advantages of the $\Delta\Sigma$ (Delta-Sigma) converter, yet is capable of offset-free and accurate conversion.*

In this conference paper, theoretical and practical aspects of higher-order incremental converters are discussed. Operating principles, topologies and specialized digital filter design methods are addressed. The theoretical results are verified by showing design examples and simulation results.

***Keywords** – mixed-signal, incremental (integrating) A/D converter, one-shot, one-cycle, no-latency converter, delta-sigma ($\Delta\Sigma$) modulator, decimating filter*

I. INTRODUCTION

Currently, high-accuracy A/D converters usually employ delta-sigma modulation. Converters designed this way are used mainly in telecommunication and consumer electronics applications, such as CD audio. In these areas, the converters are usually characterized by AC parameters, e.g. by dynamic range and signal-to-noise ratio (SNR). Moreover, these $\Delta\Sigma$ converters are mainly dedicated to applications which can tolerate offset and gain errors.

On the other hand, in instrumentation and measurement (such as digital voltmeters and sensor applications) often data converters with high *absolute* accuracy are required, and offset and gain errors cannot be tolerated. In addition, these converters need to exhibit excellent differential and integral linearity, low offset and gain errors, and they often must have high resolution and low power consumption. Thus, in these systems the spectral behaviour is of secondary importance. More important is to deliver good sample-by-sample conversion performance.

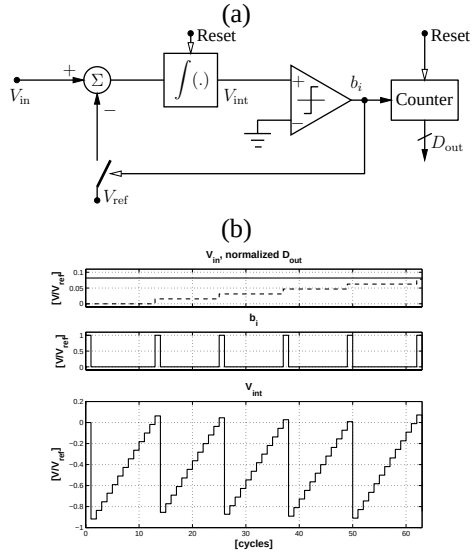

Figure 1. (a) First-order incremental converter and (b) its operation ($n = 6$ bits, $V_{\rm in} = .0818 V_{\rm ref}$).

For many years, dual-slope and voltage-to-frequency converters have dominated DC measurement applications. However, converters based on $\Delta\Sigma$ modulation can offer superior performance while requiring no external components (such as integrating capacitors). Their insensitivity to the mismatch of analog components is also a great advantage.

The incremental (or integrating) converter is capable of filling the gap between medium resolution, low-offset Nyquist-rate converters and the high resolution, high-offset $\Delta\Sigma$ converters. As an illustration, first the first-order incremental converter (Fig. 1(a)) [1] is discussed briefly.

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Its operation (which is close to that of the dual-slope principle) is as follows (Fig. 1(b)). At the beginning of a new conversion, the integrator in the loop and the output counter are both reset. Next, a fixed number (2^n) of integration steps are performed (considering a discrete-time integrator), where n is the required resolution in bits. Whenever the input to the comparator exceeds zero, its output becomes 1, and $-V_{\rm ref}$ is added to the input of the analog integrator. After 2^n steps, the output of the integrator (which is bounded by $(-V_{\rm ref}, V_{\rm in})$) becomes

$$V_{\rm int} = 2^n V_{\rm in} - N V_{\rm ref}, \tag{1}$$

where N is the number of clock periods when feedback was applied. This implies that

$$N = 2^n (V_{\rm in}/V_{\rm ref}) + \epsilon, \tag{2}$$

where $\epsilon \in [-1, 1]$. Generating N with a simple counter at the output of the modulator, one can easily get the digital representation of the input signal.

The incremental converter is structurally similar to the conventional delta-sigma ($\Delta\Sigma$) converter, but there are significant differences: (i) the converter does not operate continuously; (ii) both the analog and digital integrator are reset after each conversion; and (iii) the decimating filter following the $\Delta\Sigma$ modulator is realized with a much simpler structure (in this case, with a simple counter).

The first-order incremental converter's biggest drawback is that its conversion rate is very slow compared to its clock frequency. To reduce the number of cycles during one conversion, several improvements have been proposed [2]–[7].

Another way of extending the resolution of the incremental converters is to use higher-order single-stage modulators. Even though converters based on this structure appear to be commercially available [8]–[11], their theory and design methodology is only discussed very sketchily in the open literature (e.g. [12]–[14]).

In the following, the structure and operation of a higher-order incremental converter will be discussed.

II. OPERATION OF THE SECOND-ORDER INCREMENTAL CONVERTER

The basic block diagram of a higher-order incremental converter is shown in Fig. 2. The converter consists of a discrete-time (e.g., switched-capacitor) $\Delta\Sigma$ modulator, a digital filter and a control circuit. The operation will be discussed in terms of a second-order cascaded-integrator/feedforward modulator structure [15] shown in Fig. 3.

As for the first-order modulator, all memory elements in the analog and digital domain must be reset at the beginning of each conversion cycle. Then, $V_{\rm in}$ is applied to the input of the first integrator for the first n clock cycle. Thus, a transient operation is achieved. Using the notations of Fig. 3, the output signals of all analog integrators will next be derived in the time domain after the first n clock cycles.

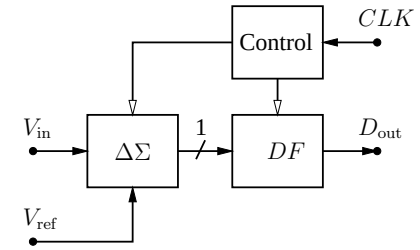

Figure 2. Block diagram of the higher-order incremental converter.

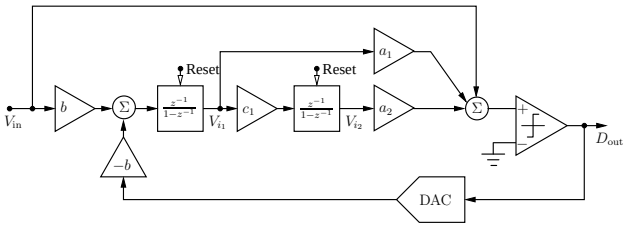

Figure 3. A second-order *Cascaded Integrator, Feed-Forward (CIFF)* architecture.

The first integrator's output samples are given by

$$\begin{aligned}
V_{i_1}[0] &= 0 \\
V_{i_1}[1] &= b(V_{\rm in}[0] - d_0 V_{\rm ref}) \\
V_{i_1}[2] &= V_{i_1}[1] + b(V_{\rm in}[0] - d_1 V_{\rm ref}) = \\
&\qquad b(V_{\rm in}[0] + V_{\rm in}[1] - d_0 V_{\rm ref} - d_1 V_{\rm ref}) \\
&\;\;\vdots \\
V_{i_1}[n] &= b \sum_{k=0}^{n-1} (V_{\rm in}[k] - d_k V_{\rm ref}),
\end{aligned} \tag{3}$$

where $d_k = \pm 1$ is the comparator output in the kth cycle.

Similarly, the sequence of outputs of the second integrator is

$$\begin{aligned}
V_{i_2}[0] &= 0 \\
V_{i_2}[1] &= c_1 V_{i_1}[0] + V_{i_2}[0] = 0 \\
V_{i_2}[2] &= c_1 V_{i_1}[1] + V_{i_2}[1] = c_1 (V_{i_1}[1] + V_{i_1}[0]) \\
V_{i_2}[3] &= c_1 V_{i_1}[2] + V_{i_2}[2] = c_1 (V_{i_1}[2] + V_{i_1}[1] + V_{i_1}[0]) \\
&\;\;\vdots \\
V_{i_2}[n] &= c_1 \sum_{l=0}^{n-1} V_{i_1}[l] = c_1 b \sum_{l=0}^{n-1} \sum_{k=0}^{l-1} (V_{\rm in}[k] - d_k V_{\rm ref}).
\end{aligned} \tag{4}$$

If the loop is stable for all possible DC inputs (which can be achieved by carefully scaling its coefficients [15], [16, Ch. 4–8]), then $V_{i_2}[n]$ in Eq. (4) is bounded by $\pm V_{\rm ref}$.

Rearranging Eq. (4),

$$-\frac{2!}{(n-1)n}\frac{1}{c_1 b}V_{\rm ref} < V_{\rm in} - \frac{2!}{(n-1)n}V_{\rm ref}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}d_k < +\frac{2!}{(n-1)n}\frac{1}{c_1 b}V_{\rm ref}, \quad (5)$$

results, assuming $V_{\rm in}$ is constant.

Thus, after n clock periods, an estimate of $V_{\rm in}/V_{\rm ref}$ can be found as

$$\frac{\hat{V}_{\rm in}}{V_{\rm ref}} = \frac{2!}{(n-1)n}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}d_k. \quad (6)$$

From the limits on the error of the estimate of $V_{\rm in}$, as given in Eq. (5), one can find the equivalent value of the LSB voltage as

$$V_{\rm LSB} = \frac{2\cdot 2!}{(n-1)n}\frac{1}{c_1 b}V_{\rm ref}. \quad (7)$$

The relative quantization error (in LSBs) of the modulator is given by

$$e_q = \frac{\hat{V}_{\rm in} - V_{\rm in}}{V_{\rm LSB}} = \frac{1}{2}c_1 b\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}d_k - \frac{1}{2}c_1 b\frac{(n-1)n}{2!}\frac{V_{\rm in}}{V_{\rm ref}}. \quad (8)$$

Hence, from Eq. (4),

$$V_{i_2}[n] = -2V_{\rm ref}e_q. \quad (9)$$

Thus, the remaining quantization error can be found in analog form at the output of the last integrator. Note that this derivation is valid only if the digital filter following the modulator is a direct realization of Eq. (6) (cf. Sec. III).

From Eq. (7) the equivalent number of bits (ENOB) can be derived as

$$n_{\rm bit} = \log_2\left(\frac{2V_{\rm ref}}{V_{\rm LSB}}\right) = \log_2\left(c_1 b\frac{(n-1)n}{2!}\right) \approx 2\log_2(n) + \log_2(c_1 b) - 1, \quad (10)$$

where $n \gg 1$ was assumed.

Note that although $V_{\rm LSB}$ and thus $n_{\rm bit}$ depends on the scaling coefficients of the analog loop, the ratio of the input signal and the reference signal is independent of them (cf. Eq. (6)). Thus, the conversion is insensitive to the accuracy errors of the realization of these coefficients.

In design, one needs to find the lowest value of n consistent with the required resolution. Clearly, the resolution increases rapidly with n, but as $b \le 1$ and $c_1 \le 1$ hold, it is inversely proportional to the values of these scale factors. In practice, however, these parameters cannot be chosen independently. The larger the number of clock periods (n) per conversion cycle is, the smaller the scaling coefficients must be, in order to avoid overloading the integrators. Thus, an optimum choice of n is necessary. It can be found in the following steps:

1. Limit the maximum allowable value of the input signal to a fraction of $V_{\rm ref}$. This is required, as higher-order structures will become unstable if the input signal is allowed to approach $V_{\rm ref}$.
2. Find an initial $n_{\rm id}$ by assuming an unscaled architecture, i.e. with $b = c_1 = 1$, using Eq. (10). (For 16-bit resolution, $n_{\rm id} = 363$ for a second-order modulator.)
3. Simulate the structure with constant $V_{\rm in}$ around the maximum allowed input for $n_{\rm id}$ cycles, and get estimates of the scale factors b, c_i from the integrators' maximum output swings.
4. Using the new scale factors, get a new estimate of n, using Eq. (10).
5. After repeating the previous two steps a few ($2 \sim 3$) times, usually neither the coefficients nor n will change significantly. At this point, the smallest allowable number of cycles n has been obtained. (For a second-order modulator, $n = 537$ clock periods are required.)

These derivations can easily be generalized to an arbitrary-order *Cascaded Integrator, Feed-Forward (CIFF)* $\Delta\Sigma$ modulator. The general expression for the ratio of $V_{\rm in}$ and $V_{\rm ref}$ of an Mth-order CIFF modulator is

$$\frac{V_{\rm in}}{V_{\rm ref}} = \frac{1}{\binom{n}{M}}\underbrace{\sum_{k_M=0}^{n-1}\sum_{k_{M-1}=0}^{k_M-1}\cdots\sum_{k_1=0}^{k_2-1}}_{M}d_k. \quad (11)$$

III. DIGITAL FILTER DESIGN

A. Direct Calculation of the Output

As discussed in the preceding Section, the conceptually simplest filter to produce the digital output of the converter is a filter implementing the formula given in Eq. (6). A straightforward approach to realize this filter is the use of the digital Cascade-of-Integrators (*CoI*) structure, which calculates directly the required multiple sums. Assuming one-bit quantization, the first stage can be realized simply with an up-down counter. All the other stages must be implemented as digital integrators with adequate register width, which can be either calculated [17] or found by simulation.

For a first-order converter, the digital output filter is also a first-order integrator, i.e., the output value contains the average of the input signal. Hence, if the total conversion period ($n \times (1/f_{\rm clk})$) is matched to the period of an incoming periodic noise source (such as line frequency disturbances), a first-order cancellation is automatically achieved. This property is similar to that of the dual-slope converter.

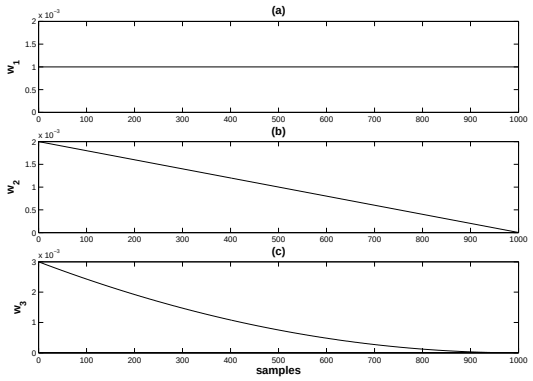

Figure 4. Weighting functions of Cascade-of-Integrators (*CoI*) filters for 1000 samples. (a) 1 integrator; (b) 2 integrators; (c) 3 integrators.

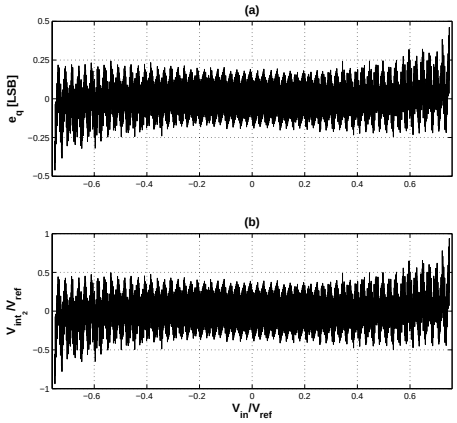

Figure 5. Simulation result of a second-order system with 10 bits resolution. (a) Quantization error; (b) Output of the second integrator (inverted).

However, in a higher-order structure, multiple integrators are used for the calculation of the output. Since the converter operates in transient mode, the digital filter can be implemented by an accumulate-and-dump structure. Hence, the final output of this filter is a weighted sum of the modulator's output samples. Fig. 4 shows the weighting functions of three digital Cascade-of-Integrators (*CoI*) filters. Clearly, due to the non-symmetrical weighting of higher-order filters, the periodic disturbances cannot be eliminated.

A first-order cancellation can be achieved, however, by including a sample-and-hold (S/H) stage at the input of the loop. If the system is operated at twice the noise frequency, and two consecutive outputs are averaged, a first-order cancellation can still be achieved. In some applications, such as control loops or multiplexed inputs, a S/H stage may be needed anyway.

Simulation results (Fig. 5) show good agreement with the discussions above. Fig. 5(a) shows the quantization error of a second-order incremental converter, calculated from the output of the second *digital* integrator (with 10-bit resolution). Clearly, the resolution is only 10 bit due to the high error peaks at large inputs. Fig. 5(b) shows the inverted output of the second *analog* integrator at the end of the conversion. It can be seen that Eq. (9) holds.

B. Filtering Using Sinc^L filters

In DC and low-frequency measurements, it is important to suppress environmental noises, especially line frequency disturbances. In this section, another filtering technique is discussed, which is able to provide adequate suppression of these noises. The proposed method can be used for first- as well as higher-order converters.

The so-called sinc^L filter [17], [18], optimized for $\Delta\Sigma$ modulators [16], [19], is the cascade of first-order averaging filters, and thus it is capable of suppressing periodic disturbances. Its transfer function is

$$H(z) = \frac{1}{M^L}\left(1 + z^{-1} + \ldots + z^{-M+1}\right)^L = \frac{1}{M^L}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^L, \quad (12)$$

where L is the order of the filter, M is the decimation ratio, $z = e^{sT}$, and $T = 1/f_s$. The free parameters of the filter are M and L. One can quickly conclude that the higher M and L are, the better the resolution and the noise suppression. However, there are some conditions which must be satisfied by these parameters.

First, if the filter is used to suppress periodic noises at the line frequency (f_l) and its multiples, then its first notch ($f_1 = f_s/M$) must be set to f_l. This leaves f_s as a variable to determine. However, too large f_s causes too tight requirements for the op-amps in the analog loop, while too small f_s causes worse thermal noise (kT/C noise) suppression of the switched-capacitor modulator.

From the derivation of Sec. II it can be seen that the order of the digital filter (L) must be at least the same as the order of the analog loop (L_a). Analysis of classical $\Delta\Sigma$ structures [19] shows that much better performance can be achieved if the order of the digital filter L is greater by one than L_a, i.e. $L = L_a + 1$. Higher-order filters will not improve the SNR any further.

Another condition on L and M is that due to the transient operation of this converter, all the registers of the digital filter must be filled with valid data to get a correct digital output. The transient length of the filter (calculated from Eq. (12)) is $N = LM - (L - 1)$. If it is realized as Cascaded Integrators and Comb-filter stages [17], its length is somewhat greater: $N = LM$. This is the minimum number of cycles the filter has to be operated for valid results.

In Sec. II, the minimum number of clock periods (n) was derived as a function of the required resolution (Eq. (10)).

However, the results were based on the Cascade-of-Integrators (*CoI*) filter structure (cf. the previous subsection). As the $\mathrm{sinc}^{\mathrm{L}}$ filter discussed here is not the optimal one, it needs more clock periods for a required resolution.

To fulfill all the above requirements, the following "cook-book" procedure is suggested:

1. Choose the analog modulator order ($L_a = 2, 3, \ldots$);
2. This determines the order of the sinc filter ($L = L_a + 1$);
3. Find $n_{\min} = n$, the required number of cycles using Eq. (10) and the iterative procedure described there; increase $n_{\min}$ until L becomes its divider;
4. Let $M = n_{\min}/L$;
5. Simulate the whole system and check the achievable resolution;
6. If the required n_{bit} resolution is not achieved, increase $n_{\min}$ with L;
7. Repeat the last two steps until the desired resolution is achieved.
8. When $n_{\min}$ and thus M is found, the clock frequency can be calculated as $f_s = M f_l$, where f_l is the line frequency.

Note that with the increase of $n_{\min}$, the scaling coefficients also have to be updated to prevent the overflow of the analog integrators. However, in practice, the algorithm is not too sensitive, and with a few iteration steps one can get good parameters for a given resolution.

Also, it should be noted that the described algorithm did not take into account the presence of thermal noise, which depends on the sampling frequency and the capacitor values of the modulator. If the size of the capacitors becomes too large with the f_s derived from the noiseless case above, then f_s must be increased until the desired SNR is achieved. In this case, the resolution limiting factor will be not the quantization error but the thermal noise.

As an example for the ideal model, $n_{\min} = 537$ is required for a second-order modulator with $u_{\max} = 0.66 V_{\mathrm{ref}}$ and 16-bit resolution. Using only second-order sinc-filter, the required number of cycles for the same resolution becomes 1092, showing the ineffectiveness of this structure. However, using third-order sinc-filter, the required number of cycles drops to $n = 576$, which is hardly larger then the ideal one, while at the same time it has the useful property of periodic noise suppression.

C. Improved Line Frequency Suppression

As discussed in the previous section, incremental converters with sinc-filters can suppress periodic noise disturbances, such as the one coming from the power line. However, in some critical applications the suppression available with simple sinc-filters may not be adequate, especially if the line frequency and/or the on-chip oscillator frequency can drift. In such cases, the zeros of the digital filter can be staggered around the notches, thus widening the frequency range around f_l, where the rejection is high.

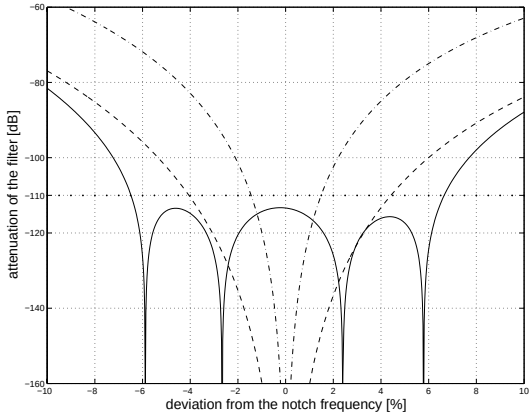

Figure 6. Transfer function of different filters around the line frequency: third-order sinc-filter (dash-dot line), fourth-order sinc-filter (dashed line) and fourth-order filter with staggered zeros (solid line).

To modify the zeros of the filter, the rotated sinc filter (RS) [20] proposed for $\Delta\Sigma$ structures can be used. A second-order factor of its transfer function is of the form

$$H_{\mathrm{dec}}(z) = \frac{1 - 2(\cos M\alpha)z^{-M} + z^{-2M}}{1 - 2(\cos\alpha)z^{-1} + z^{-2}}, \tag{13}$$

where $z = e^{j2\pi f/f_s}$ and α represents the angle of the modified complex conjugate zeros. If $\alpha = 0$, the expression simplifies to the transfer function of a second-order classical sinc filter.

For the properties of this filter and the implementation details the reader is referred to [20] and [21]. Here, only a comparison of different filtering and available rejections is discussed.

Fig. 6 compares the achievable rejection around the line frequency using various filter configurations. The dash-dot line shows the rejection of a third-order sinc-filter around the line frequency. The dashed line shows the rejection of a fourth-order sinc-filter. Finally, the solid line illustrates the rejection of the same fourth-order filter with modified zeros, and thus with widened stopband. If the required attenuation of the line frequency is -110 dB, then the third-order, fourth-order and modified fourth-order filter can obtain this attenuation in the ranges $f_l \pm 1.5\%$, $f_l \pm 4\%$ and $f_l \pm 6.5\%$, respectively.

Similar techniques can be used to suppress both $f_{l_1} = 50$ Hz and $f_{l_2} = 60$ Hz simultaneously, using the same clock frequency.

IV. COMPARISON

Table I compares several different modulators using various filters. The resolution is 16 bits, while the total number of cycles changes according to the discussions of the previous sections.

The fastest settling time is obtained when the converters are used with same-order *CoI* filter. However, if the suppression of the line frequency is also a requirement, then an Lth-order modulator with an $L + 1$st-order sinc-filter may be the right

Table I. Comparison of Higher-order Incremental Converters.

Order of Modulator	Type of Digital Filter	Resolution (Accuracy)	Total Number of Cycles
2	2 integrators	16	537
2	second-order sinc	16	1092
2	third-order sinc	16	576
3	3 integrators	16	158
3	fourth-order sinc	16	350

choice. Naturally, selecting a higher-order system in order to reduce the number of cycles affects the complexity of the analog and digital circuits, thus increasing the area and power consumption.

V. CONCLUSION

In this paper, the design theory of high-order incremental converters was discussed. A second-order system was analyzed in detail. The following results were described:

- The resolution of the higher-order incremental converter and the calculation of the the output code were derived. It was shown that, although the resolution depends on the scaling coefficients of the loop, the digital estimate of the input signal does not.
- An iterative algorithm was proposed to find the smallest n for a given resolution.
- It was shown that using the direct realization of Eq. (6) to calculate the output code, the quantization error is available in analog form at the output of the last integrator for further conversion and improved resolution.
- It was shown that the direct digital realization of Eq. (6) does not suppress periodic noise. High-order sinc filters were proposed for suppression of periodic disturbances.
- The described methods were compared, and depending on the specification, different models were proposed.

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