ENHANCING THE RESOLUTION OF INCREMENTAL CONVERTERS WITH DITHER

János MÁRKUS
Advisors: István KOLLÁR, Gábor C. TEMES

I. Introduction

Incremental converters became a useful alternative of the dual-slope analog-to-digital converters in the eighties [1]. They were developed for the measurement of DC and low-frequency signals, and used in digital voltmeters and sensor applications, where high *absolute* accuracy and low power consumption are required.

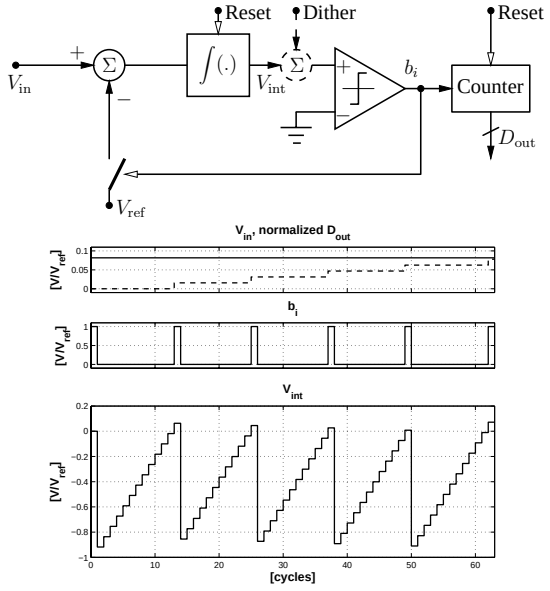

Figure 1: First-order incremental converter and its operation ($n = 6$, $V_{\rm in} = .0818$, no dither)

The unipolar first-order incremental converter (Fig. 1) is usually realized as a discrete-time switched-capacitor circuit. At the beginning of a new conversion, the integrator in the loop and the counter at the output are reset, then a fixed number (2^n) of integration steps are performed (n is the required resolution in bits). Whenever the input to the comparator exceeds zero, its output becomes 1, and $-V_{\rm ref}$ is added to the input of the analog integrator. After 2^n steps, the output of the integrator (which is bounded by $[-V_{\rm ref}, V_{\rm in}]$) becomes $V_{\rm out} = 2^n V_{\rm in} - NV_{\rm ref}$, where N is the number of cases when feedback were applied. This implies that $N = 2^n(V_{\rm in}/V_{\rm ref}) + \epsilon$, where $\epsilon \in [0, 1]$. Counting this N with a simple counter at the output of the modulator, one can easily get the digital representation of the input signal. The converter requires only simple digital circuitry, needs no precision components, and can easily be extended to bipolar operation [1].

The incremental converter is structurally based on the classical delta-sigma ($\Delta\Sigma$) converter, but there are significant differences: (i) the converter does not operate continuously, (ii) both the analog and digital integrator are reset after each conversion, and (iii) the decimating filter following the $\Delta\Sigma$ modulator is replaced with a different (easier) structure (in this case a simple counter is used).

The first-order incremental converter's biggest drawback is that for n bit resolution it needs 2^n clock periods in each conversion cycle. This leads to a very slow operation compared to its clock frequency.

The resolution of the converter (or the speed of the operation) can be improved either using higher-order modulator structures (see e.g. in [2]), or using higher-order digital filtering and appropriate dither. This latter solution is discussed below.

II. Decimation Filters

Usually $\Delta\Sigma$ modulators use sinc^l-type filters for low-pass filtering and decimating the modulated signal. It can be proven that using $l = k + 1^{\rm st}$-order filtering, where k is the order of the modulator, the output signal-to-noise ratio (SNR) does not decrease [3]. However, [2] suggests to use only $k^{\rm th}$-order filtering for the incremental converter. It was also shown that using higher-order filtering, although the

resolution and the average accuracy increased, the quantization error around zero remained the same (Fig. 2(b)). This performance degradation is due to the fact that in case of a small DC input signal the linearized models of the quantizer and the modulator are not valid any more.

III. Application of the Dither Signal

This higher quantization error around zero can be eliminated using proper dither signal in the incremental converter. Examining converters for digital voltmeters, [4] used self-subtracting and high-pass filtered external dither with 10–30 LSB amplitude added to the input signal. The solution needed external circuitry to generate and to synchronize the dither with the modulator.

This paper suggests the use of a dither signal injected into the loop, right before the quantizer (Fig. 1). This solution has several advantages including that the dither signal is shaped by the noise transfer function the same way as the quantization error, so it automatically becomes high-pass filtered. For effective dithering, relatively high amplitude is needed for the injected dither signal, causing a few dB dynamic range degradation of the input signal.

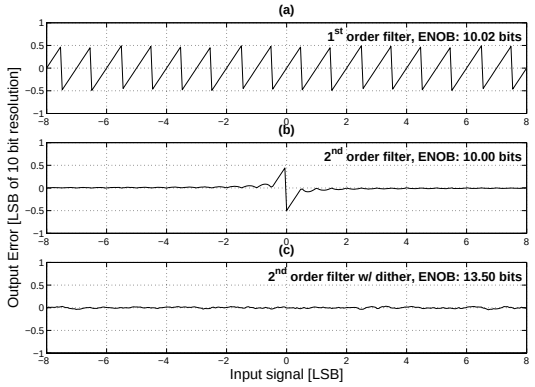

Figure 2: Quantization error of a 1st-order converter around zero input.

To verify the proposed technique, a 10-bit 1st-order converter was simulated by means of MATLAB. The quantization error of the different configurations can be seen in Fig. 2, where ENOB stands for *Effective Number of Bits*. In the first case (Fig. 2(a)), the filter is a simple counter, and the error of the output signal is similar to that of a Nyquist-rate converter. Fig. 2(b) shows the output of the same converter, using 2nd-order sinc-filtering. Even though the resolution increased, the accuracy around zero remained the same. Applying uniform dither signal in the loop with a relative maximum of 0.5, this problem can be eliminated. The resolution of the converter with the same number of clock cycles can be increased by 3.5 bits ($21\,\mathrm{dB}$), without modifying the analog hardware significantly (Fig. 2(c)). In other words, instead of using a 1st-order converter with $2^{13} = 8192$ cycles to get 13 bit resolution, it is enough to operate the same converter for less than $2^{10} = 1024$ cycles.

IV. Conclusion

A possible way of enhancing the resolution of incremental converters was introduced in this paper. It was shown that applying dither signal in the feedback loop and using higher-order filtering in the digital domain, the resolution can be significantly improved. The proposed technique can also be extended for higher-order structures.

References

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