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A Low-Power 22-bit Incremental ADC with 4 ppm INL, 2 ppm Gain Error and 2 μV DC Offset

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Abstract:

A low-power 22-bit incremental ADC, including an on-chip digital filter and a low-noise/low-drift oscillator, was realized in a 0.6-μm CMOS process. It incorporates a novel offset-cancellation scheme based on fractal sequences, a novel high-accuracy gain control circuit, and a novel reduced-complexity realization for the on-chip sinc filter. The measured output noise was 0.28 ppm (2.8 $\mu V_{\rm RMS}$), the dc offset 2 μV, the gain error 2 ppm, and the INL 4 ppm. The chip operates with a single 2.7 – 5 V supply, and draws only 125 μA current during conversion.

1. Introduction

Analog-to-digital converters (ADCs) used in instrumentation and measurement (I&M) applications often require very high absolute accuracy and linearity, and very low offset and noise. On the other hand, the frequency band of the input signal is usually only a few Hertz wide. Low power is also an important consideration. Typical applications include weight scales, as well as humidity, pressure or temperature sensors, and digital voltmeters.

Such I&M specifications are not easily satisfied with conventional delta-sigma ADCs, since these do not provide accurate gain and low offset, and require complex digital filters for high-accuracy performance. Dual-slope ADCs, on the other hand, are capable of low-offset and accurate gain operation, but require a very long conversion time, and are sensitive to element nonidealities.

The properties of incremental data converters (IDCs) [1] are, by contrast, well matched to the requirements of I&M. They can be considered to be delta-sigma ADCs operated in a transient mode. They provide very precise conversion with accurate gain, high linearity and low offset, and the conversion time can be relatively short. IDCs need only simple digital postfilters, and they can readily be multiplexed between multiple channels.

Earlier works, coauthored by some of the present writers, described a first-order [1] and a second-order [2] IDC. The theory of higher-order IDCs was also discussed in [3]. This paper describes a third-order IDC fabricated in a 0.6-μm CMOS process. It incorporates a novel "fractal" offset cancellation, a novel signal-scaling circuit, and a nov el on-chip realization of the digital filter. The measured data

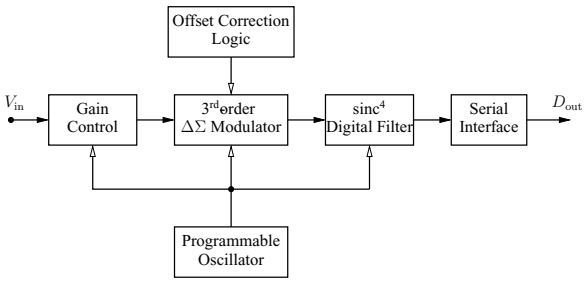


Figure 1: System diagram of the incremental data converter.

confirmed 22-bit performance, with an INL below 4 ppm, an input-referred noise below 3 $\mu V_{\rm RMS}$, and a gain error typically around 2 ppm. The measured dc offset was around 2 μV. (Note that in the paper we defined error in ppm $= 10^6 \cdot {\rm error}/2V_{\rm ref}$, as usual in the literature on I&M data converters.)

2. Architecture and Operation

Figure 1 shows the system diagram of the IDC. The input signal $V_{\rm in}$ is sampled and scaled by the precision gain control block, and then entered into a third-order low-distortion single-bit delta-sigma loop [4]. The output bit stream enters a fourth-order sinc filter [3]. The 24-bit output of the filter (22 bits of data plus two overflow bits) is the desired digital equivalent of $V_{\rm in}$. Note that the IDC is functional only for a limited number N of clock cycles. The minimum value of N is determined by two conditions: the first insures the required accuracy of the delta-sigma modulator output signal, and the second the filling of the sinc filter with data [3]. The latter condition requires $N \geq 4{\rm OSR}$, where OSR is the oversampling ratio of the modulator, and is usually the decisive condition. After N cycles, the output word is stored, and the system is reset. (In our ADC, ${\rm OSR} = 512$ and $N = 2,048$ were chosen.)

The crucial offset compensation function is controlled by the offset control logic. This controls the switches in the switched-capacitor (SC) integrators of the delta-sigm a loop so as to implement a fractal sequence. As discussed later, this involves the periodic inversion of the offset po-

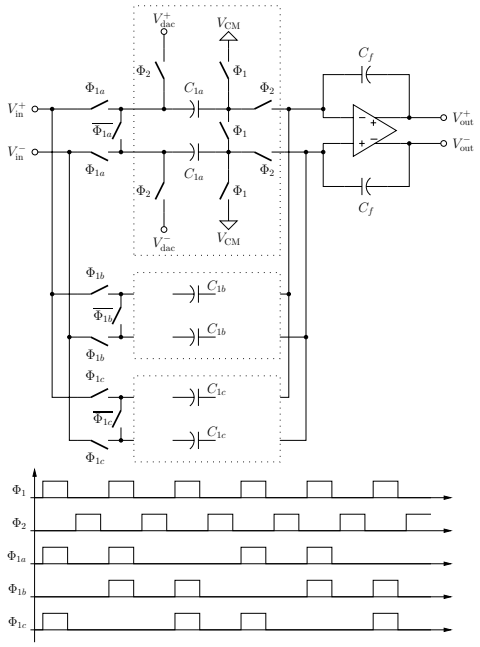


Figure 2: Gain control stage.

larity in the loop filter, and results in the cancellation of the input offset after N cycles.

The sinc filter uses a novel implementation of the familiar Hogenauer structure [5], which contains a cascade of integrating, differentiating and scaling stages. In our implementation, the differentiating stages are replaced by a programmable counter [6]. This reduces the complexity of the filter hardware.

The clock signals are provided by an on-chip relaxation oscillator, with digital frequency and temperature coefficient control. It consumes only around 50 μW power.

The operation and circuitry of the main blocks of the system are briefly discussed next.

3. The Gain Control Stage

To prevent the overloading of the delta-sigma loop, the input signal needs to be attenuated by a suitable factor. Since the IDC (unlike most conventional delta-sigma ADCs) must provide accurate gain along with high linearity, the gain reduction must be realized by a circuit which is insensitive to the inaccuracy of its components. The actual circuit implemented a factor $2/3$. It is illustrated in Fig. 2, along with its clock waveforms. In a full clock period, all three capacitors in each input branch deliver a charge proportional to the DAC voltage $V_{\rm dac}$, but only two deliver a charge proportional to $V_{\rm in}$. This provides the desired scaling. The role of the three capacitors is rotated in every clock period, thus converting the effects of mismatch errors from a gain error into an out-of-band periodic noise. This "rotating capacitor" scheme was shown to limit the gain error to a few ppm. (US patent pending.)

4. The Delta-Sigma Modulator

Figure 3 shows the simplified schematic diagram of the third-order delta-sigma modulator, without the gain- and offset-control circuits. It uses a low-distortion configuration, in which the SC integrators (ideally) do not carry the input signal, so that the required linearity of the opamps is reduced [4]. Since the input signal of an IDC is effectively dc, the oversampling ratio OSR was defined as the ratio of the loop's clock frequency f_s divided by the main notch frequency f_n of the sinc filter. In this converter, the main notch can be either $f_n = 50$ Hz or 60 Hz for line noise suppression (or $f_n = 55$ Hz for simultaneous rejection), and $\mathrm{OSR} = 512$ was used. As discussed earlier, the circuit requires $4\mathrm{OSR} = 2,048$ clock periods for converting an input sample.

The input capacitors were chosen to be 5 pF each, to keep thermal noise at a sufficiently low level.

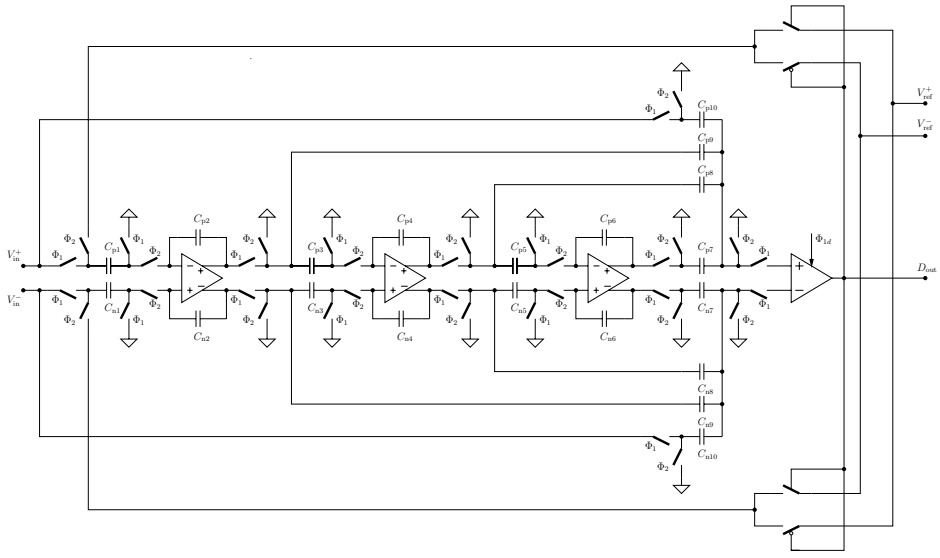


Figure 3: Simplified schematic diagram of the delta-sigma lo op.

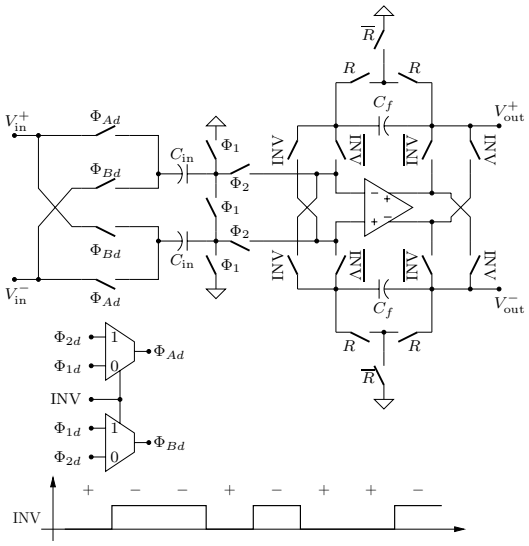


Figure 4: Switchedcapacitor integrator with signal inversion and reset switches. Subscript d indicates delayed clock phases.

5. Offset Correction

The inherent offset of the deltasigma loop must be corrected with a very high accuracy, so that the residual offset is less than 10 μV. This cannot be achieved using chopper stabilization, which is only effective for a firstorder loop. Also, correlated double sampling would have required an extra clock phase in this application. Hence, the offset correction used in this device was a generalized version of chopper stabilization, which we named "fractal sequencing." A -1 in the fractal sequence represents an inversion in the propagation path of the dc offset, while a $+1$ indicates no inversion. The signal is always integrated without any inversion. The firstorder fractal sequence S_1 is simply an alternation $+1,-1,+1,-1,\ldots$, which can be represented by the symbol $(+-)$. The secondorder sequence is then $S_2 = ((+-)(-+))$, and the thirdorder one is $((+--+)(-++-))$. In general, an $(m+1)$st order sequence S_{m+1} is obtained from an $m$thorder one S_m by concatenating S_m and the complement of S_m in which $+$ and $-$ are interchanged. It can be proven that by determining the offset propagation polarities in a cascade of m integrators according to sequence S_m, the offset at the output of the last integrator can be cancelled after the N clock periods needed for the conversion, if $N/2^m$ is an integer. Fig. 4 illustrates how the inversions in the offset path can be carried out in a differential integrator by swapping the polarities of the input and output terminals whenever the logic signal INV (controlled by S_m) is high. To keep the signal flow unchanged, the nonoverlapping phases of the four input switches are also interchanged when INV is high. (US patent pending.) The figure also shows the switches (operated by phase R) required for resetting the circuit after the Nth period.

In this device, the thirdorder fractal sequence S_3 was used, with each polarity held for 64 clock periods between inversions. The resulting $8 \cdot 64 = 512$ element pattern was repeated 4 times during the $2,048$ clock periods of operation.

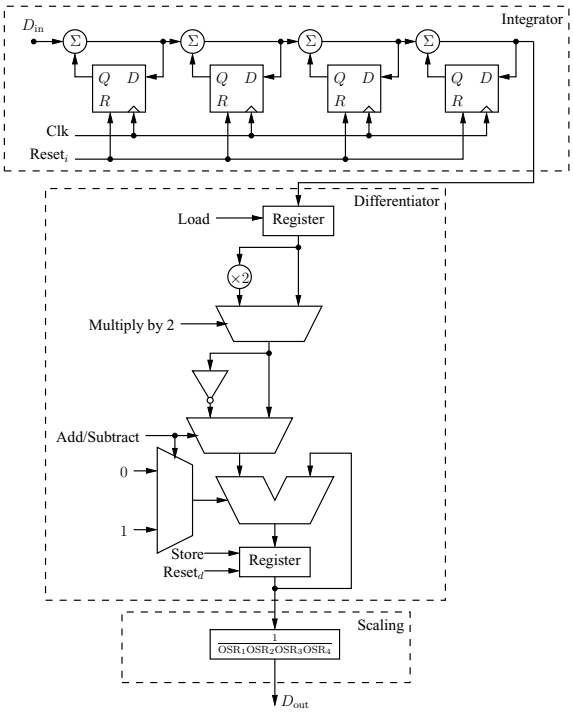


Figure 5: Block diagram of the digital postfilter.

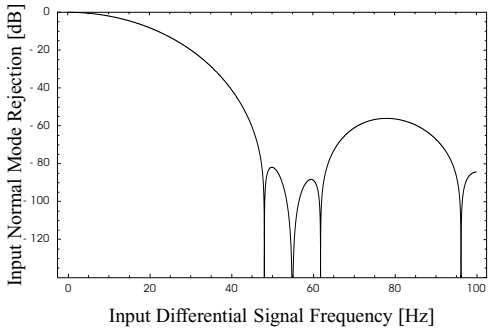
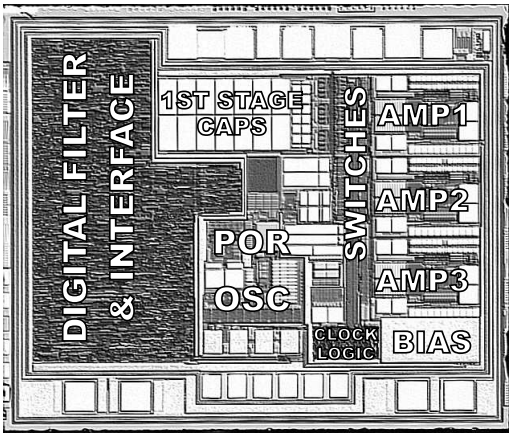


Figure 6: The gain response of the narrowband digital filter.

6. The Digital Filter

The fourthorder digital sinc filter used in the chip uses multiple staggered zeros around each notch frequency, to allow for drift in the clock rate or the line frequency. It has a modified transfer function including the staggered zeros, and uses a novel implementation [6] which differs from the familiar Hogenauer structure [5]. It utilizes a programmable counter in place of the four cascaded differentiators needed in the Hogenauer scheme. The filter contains a control unit which stores the zeros, and it operates the counter so as to implement these zeros. It provides a high noise rejection, and needs only a low complexity circuitry. The block diagram of the filter is shown in Fig. 5. Fig. 6 shows the gain response of the filter with notches around 50 and 60 Hz.



POR: Power-On-Reset

Figure 7: Chip photomicrograph.

7. Measurement Results

Three different versions of the complete ADC were implemented in a 0.6-μm CMOS technology. The first one has a slow maximum data rate (13.75 Hz), with a digital filter which rejects both 50 and 60 Hz with a wide multiple notch at 55 Hz. It has low output noise (0.28 ppm). The second chip also has a slow data rate (12.5 Hz or 15 Hz), with a greater rejection of either 50 or 60 Hz, a main notch at 50 or 60 Hz, and also low output noise (0.28 ppm). The third chip has a maximum data rate of 60 Hz, a notch at 240 Hz, and an elevated (0.8 ppm) output noise. The chip photo for the third version is shown in Fig. 7. It occupies an area of 1.59×1.31 mm^2. The measured performance is summarized in Table 1.

Table 1: Summary of the measured performance of the incremental ADC.

Parameter	Performance
DC offset	
typ.	2 μV
max.	10 μV
Gain Error†	
typ.	2 ppm
max.	10 ppm
INL†	
$V_{\rm ref} = 2.5$ V	max. 4 ppm
$V_{\rm ref} = 5$ V	max. 12 ppm
Supply Current	
Shutdown mode	max. 1 μA
Op. mode $V_{\rm DD} = 5$ V	typ. 125 μA
Op. mode $V_{\rm DD} = 3.3$ V	typ. 105 μA
CMRR‡ @ 50/60 Hz	at least 130 dB
DC PSRR‡	
$V_{\rm DD} = 2.5 \sim 6$ V	at least 120 dB
Output Noise†	
$V_{\rm ref} = 5$ V	0.28 ppm (2.8 $\mu V_{\rm RMS}$)
$V_{\rm ref} = 2.5$ V	0.48 ppm (2.4 $\mu V_{\rm RMS}$)
Oscillator frequency variation over $V_{\rm DD}$ and temperature range	$\pm 0.5\%$

† ppm of $2V_{\rm ref}$
‡ $V_{\rm in}^+ = V_{\rm in}^- = V_{\rm ref}/2$

8. Conclusions

The design and implementation of a 22-bit incremental data converter was described. It incorporates several novel algorithms and circuit techniques. The measured performance confirmed a very low offset and noise, as well as an accurately controlled gain, combined with a low power drain. Hence, the converter is suitable for high-precision instrumentation and measurement applications.

Acknowledgment

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