Incremental Delta-Sigma Structures for DC Measurement: an Overview

(Invited Paper)

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***Abstract*— In this paper the theoretical operation of incremental (charge-balancing) delta-sigma ($\Delta\Sigma$) converters is reviewed, and the implementation of a 22-bit incremental A/D converter is described. Two different analyses of the first-order incremental converter are presented, and based on these results two extensions to higher-order modulators are proposed. Since line-frequency noise suppression is often important in measurement applications, modulators followed by sinc^k filters are also analyzed. Equations are derived for the estimation of the required number of cycles for a given resolution and architecture. Finally, the design and implementation of a third-order incremental converter with a fourth-order sinc filter is briefly discussed.**

I. Introduction

Delta-Sigma ($\Delta\Sigma$) analog-to-digital converters are widely used in telecommunication and multimedia applications. The key property of these converters is that they do not rely on precisely matched analog elements to achieve high resolution, but on oversampling, noise-shaping and digital post-filtering. Thus, these converters can be integrated well into today's fine line-width CMOS technologies. The theory and operation of these converters is discussed in detail in, e.g., [1].

Unfortunately, these classical $\Delta\Sigma$ structures are not well suited for instrumentation and measurement (I&M) applications, in which very high absolute accuracy and linearity, and very low offset and gain errors are required, in addition to high dynamic range and signal-to-noise ratio. In battery-operated applications (such as smart sensors, portable weight scales, or digital multimeters) low power consumption may also be critical. On the other hand, the frequency band of the input signal is usually very narrow, often only a few Hertz wide.

In summary, in telecommunication applications usually a running waveform needs to be digitized, and mainly the output's spectral properties are important, while in I&M applications an accurate sample-by-sample mapping, as well as very good INL performance are required.

Incremental data converters (IDCs) [2], [3], which can be considered delta-sigma data converters in transient mode, are well matched to the requirements of I&M. They can provide precise high-resolution conversion with low offset and gain errors. For higher-order structures, the conversion time can be relatively short [3], [4]. For the measurement of dc input signals, IDCs need only simple digital postfilters. Since the operation of such converters is intermittent, they can be also readily multiplexed between multiple channels.

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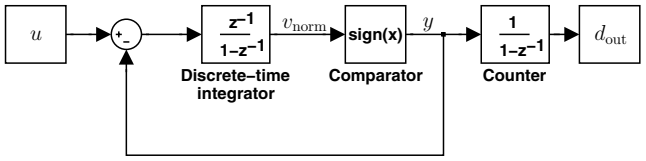

Fig. 1. Discrete-time model of a first-order bipolar incremental converter. In this model u is the normalized input signal, $v_{\rm norm}$ is the normalized output of the discrete-time integrator, $y \in \{-1, 1\}$ is the normalized feedback signal (a single-bit output sequence), while $d_{\rm out}$ is the output of the digital integrator.

This paper gives an overview of the theory and design of incremental data converters. The first part of the paper (Secs. II–IV) discusses the theoretical operation of such architectures, while the second part (Sec. V) describes the design, implementation and measured results of a low-power 22-bit IDC containing a third-order $\Delta\Sigma$ modulator. The converter exhibited a 22-bit performance with an INL below 4 ppm, an input-referred noise below 3 $\mu{\rm V}_{\rm RMS}$, a gain error typically around 2 μV, and dc offset around 2 μV.

II. First-Order $\Delta\Sigma$ A/D Converter for DC Signals

A discrete-time model of a first-order converter processing both positive and negative signals ("bipolar ADC") is shown in Fig. 1.

The operation of the converter [2] is as follows: before a new conversion, all memory elements, i.e., the switched-capacitor (SC) integrator in the loop and the digital counter at the output, are reset. Next, a fixed number ($N = 2^{n_{\rm bit}}$) of integration steps are performed. Here $n_{\rm bit}$ is the final resolution in bits. In each cycle, depending on the sign of the output of the SC integrator, the loop feeds back either a $+V_{\rm ref}$ or a $-V_{\rm ref}$ signal to the

input of the integrator.

The exact behavior of this architecture can be analyzed in two different ways. One is to use time-domain analysis to derive the output signal ($v_{\rm norm}$) of the internal integrator at cycle n. Another way is to use z-domain analysis, then return to the time domain and find the quantization error. Since these two analyses result in two different higher-order extensions of the original first-order converter, they are performed briefly in the next two subsections. Throughout the derivations, normalized signals are used, i.e., all analog signals are scaled by the reference level $V_{\rm ref}$.

A. Analysis of the Output of the Integrator in the Time-Domain

The output of the delaying SC integrator ($v_{\rm norm}$) in time step n equals the accumulated sum of its input which is the difference of the input signal $u[i]$ and the feedback signal $y[i]$:

$$v_{\rm norm}[n] = \sum_{i=0}^{n-1} (u[i] - y[i]), \tag{1}$$

assuming $v_{\rm norm}[0] = 0$ (note that $u \in [-1, +1]$ and $y \in \{-1, +1\}$). With proper signal management (see [2] and [4, Sec. 2.1.3]), it can always be ensured that $v_{\rm norm} \in [-1, 1]$, i.e., in time step N,

$$\left| \overline{u} - \frac{1}{N} \sum_{i=0}^{N-1} y[i] \right| \leq \frac{1}{N}, \tag{2}$$

where $\overline{u}$ is the estimate of the mean value of the input signal.

Eq. 2 gives the key to performing analog-to-digital conversion with such an architecture: it shows that the error between the unknown input signal $\overline{u} = \overline{V_{\rm in}}/V_{\rm ref}$ and the sum of the known terms $y[i]$ and N is bounded by a known limit. In a bipolar analog-to-digital converter, the maximum error between the normalized input and its digital representation is LSB/2, where LSB $= 2u_{\rm max}/2^{n_{\rm bit}}$, $u_{\rm max}$ is the maximum normalized input signal ($u_{\rm max} = 1$ in this case), and $n_{\rm bit}$ is the resolution in bits. Thus, $1/N = {\rm LSB}/2 = 1/2^{n_{\rm bit}}$. This means that to achieve $n_{\rm bit}$ resolution, the converter has to be operated through $N = 2^{n_{\rm bit}}$ cycles. Note that the digital filter, which provides an estimate of the input signal, according to (2), is a discrete-time integrator, operated in transient mode. Since the input signal to this filter is a single-bit sequence, this integrator may be realized by a simple up/down counter [2].

B. Analysis in the z-Domain

The first-order incremental converter may also be analyzed using classical $\Delta\Sigma$ modulator methods. With this technique, the operation of the converter is analyzed in the z-domain, and then the result is converted back to the time-domain and finite-duration operation. To use linear system analysis, the nonlinear quantizer is modelled by an adder, which adds the appropriate quantization error ($\varepsilon[i]$, $E(z)$) to the quantizer input.

Using z-domain analysis, the output of the modulator $Y(z)$ is

$$Y(z) = z^{-1}U(z) + (1 - z^{-1})E(z), \tag{3}$$

and the final output becomes

$$D_{\rm out}(z) = \frac{z^{-1}}{1 - z^{-1}} U(z) + E(z). \tag{4}$$

Switching back to time-domain and evaluating the output at $i = n$ leads to

$$D_{\rm out}[n] = \sum_{i=0}^{n-1} u[i] + \varepsilon[i]. \tag{5}$$

Rearranging this equation, and assuming that $\varepsilon[i] = y[i] - v_{\rm norm}[i] \in [-1, +1]$ (i.e., the quantizer is not overloaded), results in an expression similar to (2):

$$\left| \overline{u} - \frac{1}{N} D_{\rm out}[N] \right| \leq \frac{1}{N}. \tag{6}$$

The main difference between the two analysis methods is that in the current case the *bounded internal quantization* error was used to obtain an upper bound on the final output quantization error, while in the previous case the *bounded output of the integrator* resulted in keeping the output quantization error under a given limit. These two conditions lead to two different extensions of the incremental converter to higher-order $\Delta\Sigma$ loops, discussed later in Sec. III.

C. Improvements of the First-Order Converter

As it was shown in the previous analysis, the first-order converter's biggest drawback is that for $n_{\rm bit}$-bit precision it requires $N = 2^{n_{\rm bit}}$ clock cycles (e.g., for $n_{\rm bit} = 16$, $N = 65,536$), which leads to a very slow conversion.

Before the discussion of IDCs based on higher-order $\Delta\Sigma$ loops (Sec. III), structures which retain the first-order loop but improve its operation are reviewed. Most of these modifications are based on the fact, that with proper signal management, the quantization error of the conversion is available in analog form at the output of the switched-capacitor integrator, i.e.,

$$v_{\rm norm}[N] = -2q, \tag{7}$$

where q is the quantization error of the output of one conversion cycle, and $v_{\rm norm}[N]$ is the normalized output of the integrator at the end of the conversion [4, Sec. 2.1.3]. This is a large signal (the analog signal swing is between $\pm V_{\rm ref}$), which can be further digitized, and the result may be used to refine the output.

The easiest way to reduce the required number of cycles for the conversion is to apply a Nyquist-rate A/D converter which takes $v_{\rm norm}[N]$ as an input signal and converts it to a digital word. This can be concatenated with the output of the IDC to obtain a more accurate result. Using the comparator already in the circuit as a single-bit A/D, the resolution may be increased by one bit, or the required number of cycles can be halved. This idea was actually utilized in the original circuit of [2]. In [5], a multibit Nyquist-rate A/D converter was placed into the circuit to convert $v_{\rm norm}[N]$ into a digital correction word. More sophisticated solutions used the same hardware to process the output of the integrator:

In [6], successive approximation was used at the end of the conversion, while [7] and [8] introduced the extended-counting principle based an algorithmic conversion, and [9] proposed a two-step algorithmic converter, resulting in very low power and reduced chip area.

Another solution to reduce the number of cycles is to use a multi-stage (MASH) incremental converter. A two-stage architecture was described in [10], reducing the required number of cycles to about $N = 2^{n_{\rm bit}/2}$. A similar solution was proposed in [11].

Another way of extending the resolution of incremental converters is to use a higher-order single-stage loop. The theory for such incremental converters utilizing a cascaded-integrators/feed-forward (CIFF) $\Delta\Sigma$ architecture has been published earlier by some of the present writers in [3]. In addition, the detailed description of a 22-bit, third-order IDC has been presented by us in [12]. Here, the theory is extended to two types of modulators based on [4, Sec. 3.2] (Sec. III), the design equations for modulators followed by sinc^k filters are given (Sec. IV), and the design of the high-resolution converter is briefly discussed (Sec. V).

III. Extensions to Higher-Order $\Delta\Sigma$ Modulators

In the previous section, two different analyses of the first-order incremental converter were given: it was shown that the bounds on either the internal quantization error or on the output of the analog integrator can be used to determine the required number of cycles (N) for a given resolution ($n_{\rm bit}$). Based on these criteria, two generalizations of the first-order converter are derived in the following.

A. Modulators with Maximally Flat Noise Transfer Function

Consider a higher-order modulator whose output is given by

$$Y(z) = z^{-k}U(z) + (1 - z^{-1})^{L_a}E(z), \tag{8}$$

where $E(z)$ is the normalized quantization error of the internal quantizer, $U(z)$ is the normalized input signal, L_a is the order of the analog modulator, and $k \le L_a$ holds. To ensure the stability of such $\Delta\Sigma$ modulator for $L_a > 2$, multibit (l-level) internal quantizer may be used [1, Chap. 4]. As the nonlinearity of the multibit feedback DAC will cause severe degradation in the performance, the DAC linearity must be improved, usually by a dynamic mismatch shaping algorithm [1, Chap. 6].

As for the first-order modulator, if $L_d = L_a$ digital integrators are applied at the output of the modulator, the final digital output will contain the sum of the L_ath integral of the unknown input signal and the last sample of the internal quantization error:

$$D_{{\rm out},L_a}(z) = \frac{z^{-k}}{(1 - z^{-1})^{L_a}}U(z) + E(z). \tag{9}$$

In the time-domain (assuming $k = 0$ for simplicity, which can always be ensured [13]) this becomes

$$D_{{\rm out},L_a}[n] = \underbrace{\sum_{k_{L_a}=0}^{n}\sum_{k_{L_a-1}=0}^{k_{L_a}}\cdots\sum_{k_1=0}^{k_2}}_{L_a} u[k_1] + \varepsilon[n]. \tag{10}$$

If the input signal is constant ($u = \overline{u}$), e.g., sampled and held using an S/H circuit, then

$$D_{{\rm out},L_a} = \binom{n + L_a - 1}{L_a}\overline{u} + \varepsilon[n]. \tag{11}$$

Note that if no S/H circuit is used in front of the converter, then the output signal $D_{{\rm out},L_a}$ is only an estimate of $\overline{u}$, but the variance of any noise on $\overline{u}$ is greatly reduced by the internal oversampling and the low-pass filtering effect of converter [3], [4, Sec. 4.1].

From this equation, proceeding as in Sec. II-B, the quantization error q of the conversion can be found:

$$q = \frac{\varepsilon[N]}{\binom{N+L_a-1}{L_a}} \le \frac{1}{(l-1)\binom{N+L_a-1}{L_a}}, \tag{12}$$

where $\varepsilon[N] \in [-1/(l-1), 1/(l-1)]$ is the quantization error of the internal l-level quantizer in time step N. The maximum quantization error must be equal to half LSB of the target resolution. Since in higher-order architectures the input signal ($V_{\rm in}$) must be limited to a fraction of the reference signal ($V_{\rm ref}$) to prevent the integrators and the internal quantizer from saturation, i.e., $V_{\rm in}/V_{\rm ref} = u \le u_{\max} < 1$, the LSB of the bipolar converter can be defined as $2u_{\max}/2^{n_{\rm bit}}$. Then, the following equality has to be fulfilled by N:

$$\frac{u_{\max}}{2^{n_{\rm bit}}} = \frac{1}{(l-1)\binom{N+L_a-1}{L_a}}, \tag{13}$$

from which the required number of cycles N for a given resolution $n_{\rm bit}$ can be found:

$$\binom{N + L_a - 1}{L_a} = \frac{2^{n_{\rm bit}}}{(l-1)u_{\max}}. \tag{14}$$

As an example, for 16-bit resolution, with a second-order architecture, assuming $l = 5$ and $u_{\max} = 0.8$, $N = 203$ results.

B. The Cascaded-Integrators, Feed-Forward Structure

As shown in Sec. II-A, the bound on the output of the (last) analog integrator may also be used to obtain the final quantization error. This method is effective for higher-order converters, however, only if the output of the last integrator does not contain the input signal itself. This property can be ensured by using the Cascaded-Integrators, Feed-Forward (CIFF) structure [14], where the input signal is also fed to the input of the quantizer [13]. A third-order CIFF example is shown in Fig. 2. In the following, a single-bit internal quantizer is assumed to avoid dealing with the problems of the multibit feedback DAC.

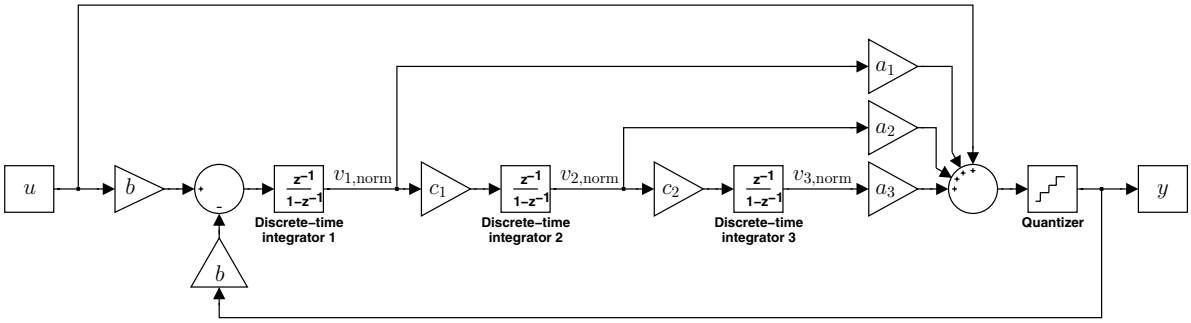

Fig. 2. A third-order *Cascaded Integrator, Feed-Forward (CIFF)* architecture with the input signal fed forward to the input of the quantizer. $\mathbf{a} = [1.4,\ 0.99,\ 0.47]$, $b = 0.5674$, $\mathbf{c} = [0.5126,\ 0.3171]$, $u_{\max} = 0.67$.

The key property of this architecture is that the signal transfer function of the modulator $STF(z) = 1$, i.e., the output of the modulator is $Y(z) = U(z) + NTF(z)E(z)$, and thus the signal entering to the integrator stages is $U(z) - Y(z) = NTF(z)E(z)$. This way, the integrators in the loop do not process the input signal, only the shaped internal quantization error. This architecture has several additional benefits [15].

The output of the last (third) integrator in the loop in time-step n is the triple sum of the difference of the input and the feedback signal multiplied by the gain factors in the loop (cf. Fig. 2) [3]:

$$v_{3,\mathrm{norm}}[n] = c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} \left(u[k] - y[k]\right). \tag{15}$$

If the loop is stabilized by appropriate feedforward gains [14], the normalized output swing of the last integrator can be kept between ± 1 by appropriately setting the c_i scaling coefficients. Then, similarly to the previous cases, there is a relation giving an upper bound on the difference of the unknown constant input signal and some known terms:

$$\left| \binom{N}{3} \overline{u} - \sum_{m=0}^{N-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} y[k] \right| \leq \frac{1}{c_2 c_1 b}. \tag{16}$$

From this, the half LSB of the target resolution may be obtained:

$$\frac{1}{c_2 c_1 b \binom{N}{3}} = \frac{\mathrm{LSB}}{2} = \frac{u_{\max}}{2^{n_{\mathrm{bit}}}}. \tag{17}$$

Rearranging this equation, the required number of cycles to achieve a given resolution can be calculated from

$$\binom{N}{L_a} = \frac{2^{n_{\mathrm{bit}}}}{u_{\max} \left(\prod_{i=1}^{L_a - 1} c_i \right) b}, \tag{18}$$

which gives an expression similar to (14). The main difference is that the number of levels in the quantizer are replaced by the gain factors of the loop. As an example, a 20-bit converter with third-order modulator and $u_{\max} = 0.67$ and with gain factors given in Fig. 2, the required number of cycles $N = 468$.

IV. Line Noise Suppression

In the previous subsections two extensions of the original first-order incremental converter were presented. In (10) and (16) the required digital filters to process the output of the modulator were also implied: in both cases, cascade-of-integrators (CoI) filters, operated in a transient mode, were required to calculate the output of the converter. The number of digital integrators (L_d) was equal to the order of the modulator (L_a).

The higher-order ADCs discussed above have a practical disadvantage compared to the first-order converter: these converters cannot provide a suppression of a periodic noise, such as 50 or 60 Hz line noise [4, Secs. 4.1.2, 4.1.3]. In some cases, suppression of the line frequency noise is essential for precise measurements in I&M applications. Then, the digital filter following the modulator has to be modified to meet this requirement. One possibility is to use a higher-order sinc^k filter [16], in which case the required number of cycles cannot be calculated anymore using (14) or (18), but can be derived as follows.

An L_dth-order sinc filter with a decimation ratio of M has the transfer function

$$H(z) = \frac{1}{M^{L_d}} \left(\frac{1 - z^{-M}}{1 - z^{-1}} \right)^{L_d}. \tag{19}$$

To design the filter, one has to find the order L_d, and the decimation (or oversampling) ratio of the filter M. M also gives the ratio between the clock rate and the first null of the transfer function. Since incremental converters are used in a transient mode, as in the previous discussions, time-domain methods can be used to find M, and thus the required number of cycles N. In the following analysis, systems with filter order $L_d = L_a$ and $L_d = L_a + 1$ are examined. It can be proven that filters with higher orders do not give optimal trade-off between the required number of cycles and circuit complexity [4, Sec. 4.2.1]. Note that when the value of M required for a given resolution is derived, it is advantageous to increase it to be a power of 2: this way, $1/M^{L_d}$ can be implemented very easily, e.g., using a shift register.

A. Modulators with Maximally Flat NTFs

1) $L_d = L_a$: Consider an L_ath-order $\Delta\Sigma$ modulator with a maximally flat NTF, followed by an L_dth-order sinc^{L_d} filter, where now $L_d = L_a = L$. In this case, the combined transfer function of the modulator and the filter becomes

$$D_{\mathrm{out}}(z) = H(z)U(z) + H(z)(1-z^{-1})^L E(z) = \\ = \frac{1}{M^L}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^L U(z) + \frac{1}{M^L}\left(1-z^{-M}\right)^L E(z), \tag{20}$$

where $H(z)$ is defined in (19). Thus, the input signal is filtered by a regular higher-order sinc filter, which does not affect the input signal at dc, and which provides periodic noise suppression at its zeros.

To find the required number of cycles for a given resolution, the largest output error has to be found, and equated to the half LSB of the target resolution. Considering a third-order structure ($L = 3$), the error at the output is given by

$$Q(z) = \frac{1}{M^L}\left(1-z^{-M}\right)^L E(z) = \\ = 1/M^3(1 - 3z^{-M} + 3z^{-2M} - z^{-3M})E(z). \tag{21}$$

The finite impulse response of this transfer function (without the scaling coefficient) is shown in Fig. 3(a). From this equation and the figure, two conclusions can be drawn: (i) to fill the digital filter with valid data, the minimum required number of cycles is $N = 3M$, and (ii) the worst-case sequence of the internal quantization error (assuming an l-level quantizer) is when the error samples take on their positive (negative) maximum value, whenever the filter coefficient is positive (negative). That is, the worst-case sequence is $\varepsilon[i] = (1, -1, 1, -1)/(l-1)$ at time steps 0, M, $2M$ and $3M$, respectively. This gives for the upper bound for the final quantization error

$$|q| \le \frac{1+3+3+1}{M^3(l-1)} = \frac{8}{M^3(l-1)}, \tag{22}$$

which must equal the half LSB of the target resolution:

$$\frac{8}{M^3(l-1)} = \frac{u_{\max}}{2^{n_{\mathrm{bit}}}}. \tag{23}$$

From this equation, M can be calculated

$$M = \sqrt[3]{\frac{8\cdot 2^{n_{\mathrm{bit}}}}{u_{\max}(l-1)}}, \tag{24}$$

and the required number of cycles is $N = 3M$.

2) $L_d = L_a+1$: Consider now the case when the modulator order is $L_a = 3$ and that of the sinc filter is $L_d = L_a+1 = 4$. In this case, the merged NTF of the system becomes

$$\frac{D_{\mathrm{out}}(z)}{E(z)} = \frac{1}{M^4}\frac{\left(1-z^{-M}\right)^4}{1-z^{-1}} = \\ = \frac{1}{M^4}\frac{1-z^{-M}}{1-z^{-1}}\left(1-z^{-M}\right)^3, \tag{25}$$

which is the product of an L_ath-order differential filter and a first-order sinc filter. The impulse response of such a filter is shown in Fig. 3(b). In this case, many samples of the internal quantization error $\varepsilon[i]$ are weighted and summed together to get the output quantization error q. Thus, statistical methods have to be used to find the statistical properties of the final quantization error. If the internal quantization error $\varepsilon[i]$ has approximately uniform distribution between $\pm 1/(l-1)$, (i.e., $m_\varepsilon = 0$ and $\sigma_\varepsilon^2 = 4\cdot 1^2/12(l-1)^2$), the output quantization error has an approximately Gaussian distribution, according to the central limit theorem. The output variance is the sum of the variances of the individual samples, weighted by the square of the filter coefficients:

$$\sigma_q^2 = \frac{4\cdot 1^2}{12M^8(l-1)^2}(M\cdot 1^2 + M\cdot 3^2 + M\cdot 3^2 + M\cdot 1^2) = \\ \frac{20}{3M^7(l-1)^2}. \tag{26}$$

Since the output error distribution is approximately Gaussian, one may estimate its lower and upper bounds as $k\sigma_q$, where $k \ge 3$. In this case, the expected maximum output error becomes

$$k\sigma_q = \frac{k}{M^{3.5}(l-1)}\sqrt{\frac{20}{3}}, \tag{27}$$

which equals to half LSB of the target resolution:

$$\frac{k}{M^{3.5}(l-1)}\sqrt{\frac{20}{3}} = \frac{\mathrm{LSB}}{2} = \frac{u_{\max}}{2^{n_{\mathrm{bit}}}}, \tag{28}$$

from which

$$M = \sqrt[3.5]{\frac{k2^{n_{\mathrm{bit}}}\sqrt{20/3}}{(l-1)u_{\max}}}, \tag{29}$$

and the required number of cycles $N = 4M$ follows. Note that simulations indicate that $k = 5$ (i.e., using a "5-sigma rule") gives correct M and N values [4, Sec. 4.2.1].

B. Modulators with CIFF Structure

As already noted in Sec. III-B, the performance of one-bit modulators is not degraded by imperfections of the feedback DAC, and hence they are often used. Thus, in this section, one-bit CIFF structures followed by sinc filters are examined. However, the analysis of such systems is more difficult in the time domain, since the stabilization of the one-bit loop is achieved by shifting the poles from $z = 0$ in the NTF, which now has an infinitely long impulse response. As before, two cases are of interest, when the loop and filter orders are the same ($L_d = L_a$), and when the filter order is higher by one than the order of the loop ($L_d = L_a + 1$). In the following, third-order modulator will be assumed.

1) $L_d = L_a$: The required number of cycles using same-order sinc filter at the output can be calculated as follows. The NTF of the system depicted on Fig. 2 is

$$NTF(z) = \frac{(1-z^{-1})^3}{D(z)}, \tag{30}$$

where $D(z)$ contains the stabilizing poles of the modulator. Combining this with the transfer function of the same-order

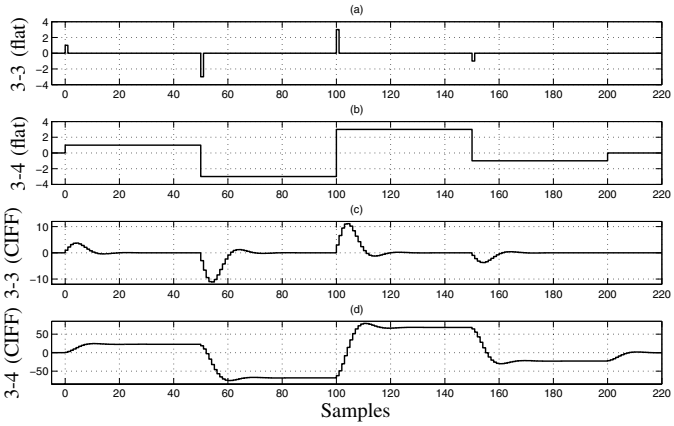

Fig. 3. Merged impulse responses of the NTF of the $\Delta\Sigma$ modulator and the sinc filter without scaling, with a decimation ratio $M = 50$. (a) third-order maximally flat modulator and third-order sinc filter (b) third-order maximally flat modulator and fourth-order sinc filter (c) third-order CIFF modulator and third-order sinc filter and (d) third-order CIFF modulator and fourth-order sinc filter.

sinc filter, the merged NTF from the internal quantizer to the output of the filter becomes

$$D_{\mathrm{out}}(z)/E(z) = \frac{1}{M^3}\frac{\left(1-z^{-M}\right)^3}{D(z)}. \tag{31}$$

A typical example of the impulse response of the merged transfer function is shown in Fig. 3(c): the response of the filter $1/D(z)$ is convolved with that of the differential response of Fig. 3(a). The required number of cycles thus $N = 3M + m$, where m is the number of samples required for the settling of the low-pass filter $1/D(z)$, while M is the decimation ratio of the sinc filter. Note that if the sinc filter is realized using the Hogenauer-structure [16], the output sample of the filter at time $3M+m$ is not available, thus one has to wait for the first valid decimated sample at time $4M$. An alternative possibility is to enlarge M, which causes smaller quantization error at the output and then ignore the error introduced by neglecting the last m samples of the transient.

To estimate the required number of samples, the bound on the output of the last integrator can be used. Due to the feed-forward structure, this signal contains only the quantization error, so

$$V_{3,\mathrm{norm}}(z) = \frac{bc_1c_2}{D(z)}E(z) < 1, \tag{32}$$

i.e.,

$$\frac{1}{D(z)}E(z) < \frac{1}{bc_1c_2} \tag{33}$$

holds. Substituting this inequality into (31) leads to

$$\frac{1}{M^3}\frac{\left(1-z^{-M}\right)^3}{D(z)}E(z) < \frac{1}{M^3}\frac{\left(1-z^{-M}\right)^3}{bc_1c_2}. \tag{34}$$

With this substitution, the problem becomes similar to the previous case (maximally flat NTF with same-order sinc filter). Using the results derived there, the bound on the maximum output error becomes

$$\frac{1}{M^3}\frac{\left(1-z^{-M}\right)^3}{D(z)}E(z) < \frac{1}{M^3}\frac{8}{bc_1c_2}, \tag{35}$$

which equals the half LSB of the target resolution ($u_{\max}/2^{n_{\mathrm{bit}}}$). This leads to

$$M = \sqrt[3]{\frac{8\cdot 2^{n_{\mathrm{bit}}}}{bc_1c_2u_{\max}}}, \tag{36}$$

and $N = 3M + m$.

2) $L_d = L_a + 1$: The last case discussed here is when a one-bit, third-order CIFF modulator is followed by a fourth-order sinc filter. In this case, the merged NTF of the system becomes

$$D_{\mathrm{out}}(z)/E(z) = \frac{1}{M^4}\frac{\left(1-z^{-M}\right)^3}{D(z)}\frac{1-z^{-M}}{1-z^{-1}}. \tag{37}$$

Its typical transient response can be seen on Fig. 3(d) (convolution of the response of Fig. 3(c) with a first-order sinc filter). Thus, the required number of cycles is $N = 4M + m$.

To find M, the bound on the output of the last integrator may again be used. Since both this signal and the final output signal contain many samples of the internal quantizer error, the statistical properties of the internal quantization error can be used to find the properties of the final output error. The output of the last integrator,

$$V_{3,\mathrm{norm}}(z) = -\frac{bc_1c_2}{D(z)}E(z) < 1, \tag{38}$$

is a stochastic variable with an approximately Gaussian distribution.

The output error distribution is also approximately Gaussian. Its variance can be readily estimated, and from it the decimation ratio required for a given resolution may be found. The result is

$$M = \sqrt[3.5]{\frac{2^{n_{\mathrm{bit}}}\sqrt{20}}{bc_1c_2u_{\max}}\sqrt{\frac{\left(\sum_{i=1}^{m} w_d[i]\right)^2}{\sum_{i=1}^{m} w_d[i]^2}}}. \tag{39}$$

Here, $w_d[i]$ is the ith sample of the impulse response corresponding to $1/D(z)$. The required number of cycles can be estimated from $N = 4M + m$.

The derivation of these results can be found in [4, Sec. 4.2].

C. Improved Line-Frequency Suppression

In critical applications, the suppression available by using the simple sinc filters may not be adequate, especially if the line frequency and/or the on-chip oscillator frequency is inaccurate. In this case, the zeros of the sinc^k filter can be staggered around the line frequency f_l, thus widening the frequency range where the rejection is high.

To modify the zeros of the filter, the rotated sinc^k filter (RS filter) introduced by Lo Presti [17] may be used. A second-order factor of its transfer function is of the form

$$H(z) = \frac{1 - 2(\cos M\alpha)z^{-M} + z^{-2M}}{1 - 2(\cos \alpha)z^{-1} + z^{-2}}, \tag{40}$$

where $z = e^{j2\pi f/f_s}$ and α represents the angle of the modified complex conjugate zeros in the z plane. If $\alpha = 0$, the expression simplifies to the transfer function of a second-order classical sinc filter. The details of the design method and optimization of this filter to suppress noise in a given region (say $f_l \pm 5\%$) can be found in [17]. Note that in the case of narrow-band filtering the angle of the zeros, α, is very small, thus $\cos(\alpha)$ is very close to 1. In this case, the number of bits in the digital word required for the accurate representation of the coefficients would be very large. To save chip area, in the implementation of this filter a different approach is used (cf. Sec. V-C).

If such an improved filter is used at the output of the modulator, it is very hard to find the required number of cycles analytically. But, since α is typically very small, the impulse response of the modified sinc filter is very similar to that of the original filter. Thus, a good estimation for M and N can be found by assuming that a simple sinc filter was used, and can be corrected if required.

V. Case Study: A Third-Order, 22-bit Incremental ADC

In this section, a brief overview of the design of a 22-bit incremental converter is given. Details of the design and performance of the converter can be found in [12].

A. Modulator Structure and Gain Control

A third-order low-distortion CIFF structure with a single-bit quantizer was chosen for the converter (Fig. 2), followed by a modified fourth-order sinc filter. For the required 22-bit resolution, (39) suggests a minimum decimation ratio $M = 353$, $m = 30$ and $N = 4M + m$, when the circuit and coefficients of Fig. 2 were used. In the actual circuit, to make the implementation of $1/M^{L_d}$ easier, $M = 512$ was used. Simulations indicated that using such M, the tail end of the transient response can be neglected without decreasing the performance, thus, in the final circuit $N = 4M$ was used. This way, the quantization error was reduced by using larger M, but the tail end of the transient response (m) could be neglected.

To prevent the overloading of the delta-sigma loop, but yet to allow the input signal to reach $\pm V_{\mathrm{ref}}$, the input signal needed to be attenuated by a suitable factor. Since the IDC (unlike most conventional delta-sigma ADCs) must provide accurate gain along with high linearity, the gain reduction must be realized by a circuit which is insensitive to the inaccuracy of its components. This can be achieved by using n_c capacitors at the input stage, out of which only $m_c < n_c$ is used to sample the input signal and n_c are used to sample the feedback signal, thus realizing a scaling by m_c/n_c of the input signal. To convert the gain error introduced by the mismatch of the scaling circuit to an out-of-band periodic noise, in every clock cycle different m_c capacitors are selected to sample the input signal. The details of this scheme can be found in [12].

B. Offset Correction

The inherent offset of the delta-sigma loop must be corrected with a very high accuracy, so that the residual offset is less than 10 μV. This cannot be achieved using chopper stabilization, which is only effective for a first-order loop. Correlated double sampling can also be used for offset suppression, but it would have required an extra clock phase in this application. Hence, the offset correction used in this device was a generalized version of chopper stabilization, which was named "fractal sequencing." Here, the propagation path of the dc offset is inverted during conversion, controlled by a sequence which provides offset correction for an arbitrary number of cascaded integrator stages. The details of this technique can also be found in [18] and [12].

C. Digital Filter Realization

The fourth-order digital sinc filter used in the chip uses multiple staggered zeros around each notch frequency [17], to allow for drift in the clock rate or the line frequency. It has a modified transfer function including staggered zeros, and uses a novel implementation which differs from the familiar Hogenauer structure [16] and also from the one suggested by [17]. It utilizes a programmable counter in place of the four cascaded differentiators needed in the Hogenauer scheme. The filter contains a control unit which stores the zeros of $H(z)$, and it operates the counter so as to implement these zeros. It provides a high noise rejection, and needs only a low complexity circuitry. Details about the filter implementation can be found in [19] and [12].

D. Implementation and Measurement Results

Three different versions of the complete ADC were implemented in a 0.6-μm CMOS technology. The first one has a slow maximum data rate (13.75 Hz), and includes a digital filter which rejects both 50 and 60 Hz with a wide multiple notch at 55 Hz. It has low output noise (0.25 ppm). The second chip also has a slow data rate (12.5 Hz or 15 Hz), a main notch at either 50 or 60 Hz, with greater rejection (at least 120 dB within a 3% variation from the selected

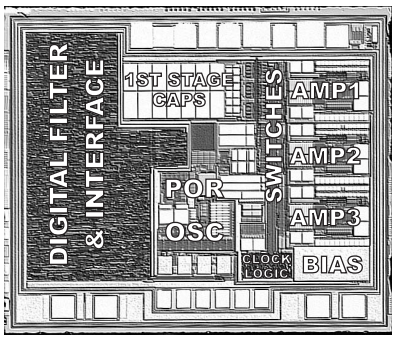

Fig. 4. Chip photomicrograph (POR: Power-On-Reset)

TABLE I

MEASURED PERFORMANCE OF THE INCREMENTAL ADC

Parameter	Performance
Conversion time	
typ.	66.7 ms
DC offset	
typ.	2 μV (1.7 LSB)
max.	10 μV (8.4 LSB)
Gain Error†	
typ.	2 ppm (8 LSB)
max.	10 ppm (40 LSB)
INL†	
$V_{\rm ref} = 2.5$ V	max. 4 ppm (16 LSB)
$V_{\rm ref} = 5$ V	max. 10 ppm (40 LSB)
Supply Current	
Shutdown mode	max. 1 μA
Op. mode $V_{\rm DD} = 5$ V	typ. 120 μA
Op. mode $V_{\rm DD} = 3$ V	typ. 100 μA
CMRR‡ @ 50/60 Hz	at least 135 dB
DC PSRR‡	
$V_{\rm DD} = 2.5 \sim 6$ V	at least 120 dB
Output Noise†	
$V_{\rm ref} = 5$ V	0.25 ppm (2.5 $\mu V_{\rm RMS}$, or 1 LSB)
$V_{\rm ref} = 2.5$ V	0.48 ppm (2.4 $\mu V_{\rm RMS}$, or 2 LSB)
Oscillator frequency variation over $V_{\rm DD}$ and temperature range	$\pm 0.5\%$

† ppm of $2V_{\rm ref}$. 1 ppm = 4 LSB
‡ $V_{\rm in}^+ = V_{\rm in}^- = V_{\rm ref}/2$

line frequency), and also low output noise (0.25 ppm). The third chip has a maximum data rate of 60 Hz, a notch at 240 Hz, and an elevated (0.8 ppm) output noise. These three versions differed in their clock frequencies, decimation ratios, and in the locations of the zeros implemented by the digital filter. Details on the implementation of the switched capacitor integrators can be found in [12]. The chip photo for the third version is shown in Fig. 4. It occupies an area of 1.59×1.31 mm^2. The measured performance is summarized in Table I. Detailed measurement results and graphs can be found in [12].

VI. CONCLUSION

In this paper the design theory of higher-order incremental converters was discussed, and the implementation of a 22-bit converter was briefly reviewed. Two different analyses of the first-order incremental delta-sigma converter were presented, and based on these, two extensions of the converter to higher-order modulators were proposed. Since line frequency suppression is often important in measurement applications, a detailed analysis was given for modulators followed by sinc filters which allow the suppression of narrow-band noise. Design formulas for estimating the required number of clock cycles for a given resolution were given for various combinations of the modulators and filters. Finally, the implementation and measurement results of a third-order converter with a fourth-order modified sinc filter were briefly described.

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