Technical Comments

- **To switch to full-screen, use the option** `View` $\longrightarrow$ `Full Screen`**, to leave, hit the** `<Esc>` **key;**
- **If some superscript is blocked out by a gray box in the following equation:** $(x+y)^{(a_i-b_{i+1}+c_{i-1})^{(2+e^{x+a})}}$**, then uncheck the** `Edit` $\longrightarrow$ `Preferences` $\longrightarrow$ `Display` $\longrightarrow$ `Use Greek Text` **option;**
- **Mouse-click does not advance the pages. Use** `PgUp`**,** `PgDn` **or the** `arrow` **keys;**
- **Put the mouse-pointer into one of the corners, otherwise it can be annoying when it shows up at page-advancing.**

An Efficient $\Delta\Sigma$ Noise-Shaping Architecture for Wideband Applications

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− **Stability issues;**
− **Not efficient for low oversamping ratio values ($OSR = \frac{f_s}{2BW}$), e. g. 0.6 bit/order improvement for $OSR = 4$ using 1-bit quantizer.**

Multistage Modulators

+ Relies on cancellation of errors, not only noise shaping;
+ Low order (reduced analog complexity);
+ Stability can be easily achieved;
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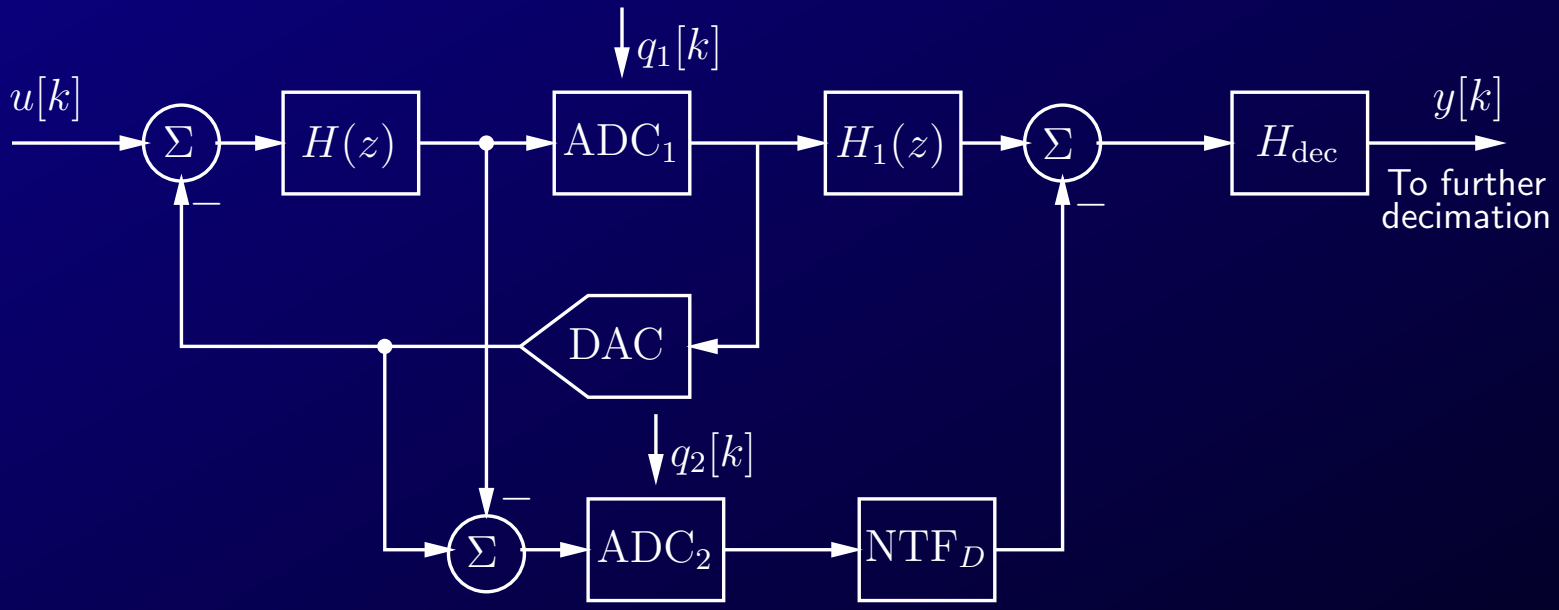
+ Second stage can be pipeline ADC;
– Mismatch problems between stages – adaptive equalization can help.

The Leslie–Singh Architecture



- $Y(z) = H_1(z)H_{\mathrm{dec}}(z)U(z) + NTF_D H_{\mathrm{dec}}(z)Q_2(z)$;
- **2nd-stage multibit ADC is operated at the same oversampling rate as the 1st stage.**

The Leslie–Singh Architecture (Cont.)

$$Y(z) = H_1(z)H_{\mathrm{dec}}(z)U(z) + NTF_D H_{\mathrm{dec}}(z)Q_2(z),$$

where

- $H_1(z)$ **is usually a delay factor;**
- $H_{\mathrm{dec}}(z)$ **is the transfer function of the first stage of the decimation filter;**
- NTF_D **is the digital replica of the noise transfer function (**NTF**) of the first stage of the modulator.**

Mth-Order Modulator

- **For Mth-order $H(z)$, usually**

$$NTF_D(z) = (1 - z^{-1})^M$$

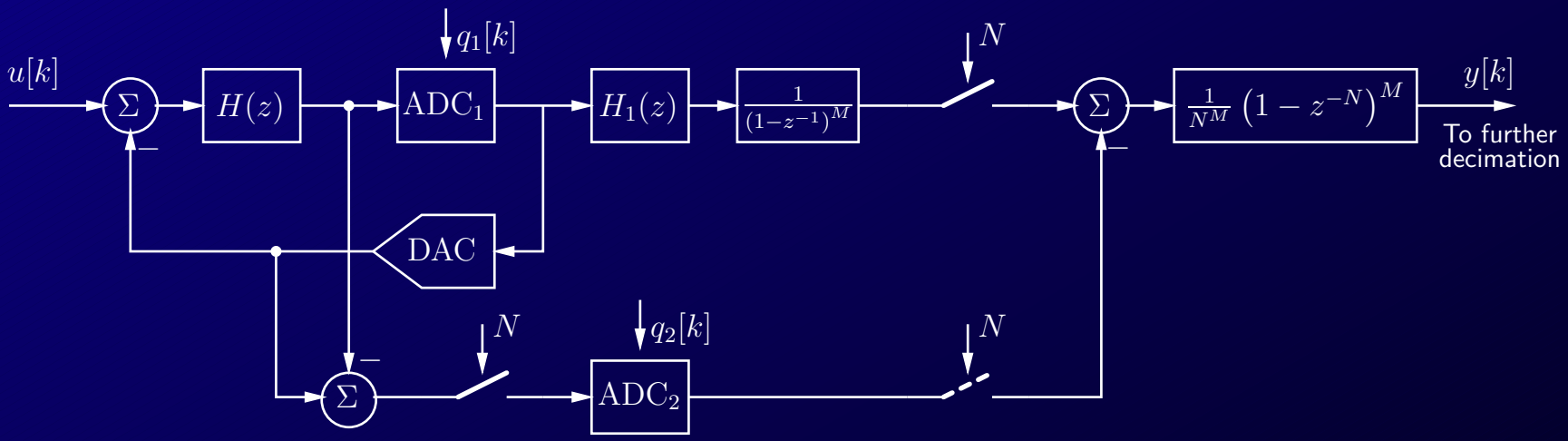
$$H_{\text{dec}}(z) = \frac{1}{N^{M'}} \frac{(1 - z^{-N})^{M'}}{(1 - z^{-1})^{M'}}$$

- **Usually $M' = M + 1$ [Candy86];**
- **If $M' = M$ is used instead, then**

$$Y(z) = H_1(z) H_{\text{dec}}(z) U(z) + \text{num}\left[H_{\text{dec}}(z)\right] Q_2(z)$$

leads to a reduced-sample-rate architecture [Qin99].

Reduced-Sample-Rate (RSR) Architecture [Qin99]



- \+ **2nd-stage multibit ADC_2 works at a lower rate;**
- \+ **Slower ADC_2 $\Rightarrow$ less power, less chip area;**
- $-$ **$M' = M$ $\Rightarrow$ Noise folds back to the baseband (3 dB loss of SNR/octave) [Candy86].**

Optimized Transfer Function

- **Use Rotated Sinc filter for decimation [LoPresti00]:**

$$H_{\mathrm{dec}}(z) = \frac{1 - 2(\cos N\alpha)z^{-N} + z^{-2N}}{1 - 2(\cos \alpha)z^{-1} + z^{-2}};$$

- **Optimize α to minimize the noise power in the output (assuming white-noise q_2);**
- **Modify the NTF_D cancelled by the denominator of the decimation filter;**
- **Modify the NTF cancelled by NTF_D.**

Optimization of α

From

$$\min_{\alpha} \int_0^{\frac{f_s}{2OSR}} |\mathrm{num}(H_{\mathrm{dec}})|^2 \, df =$$

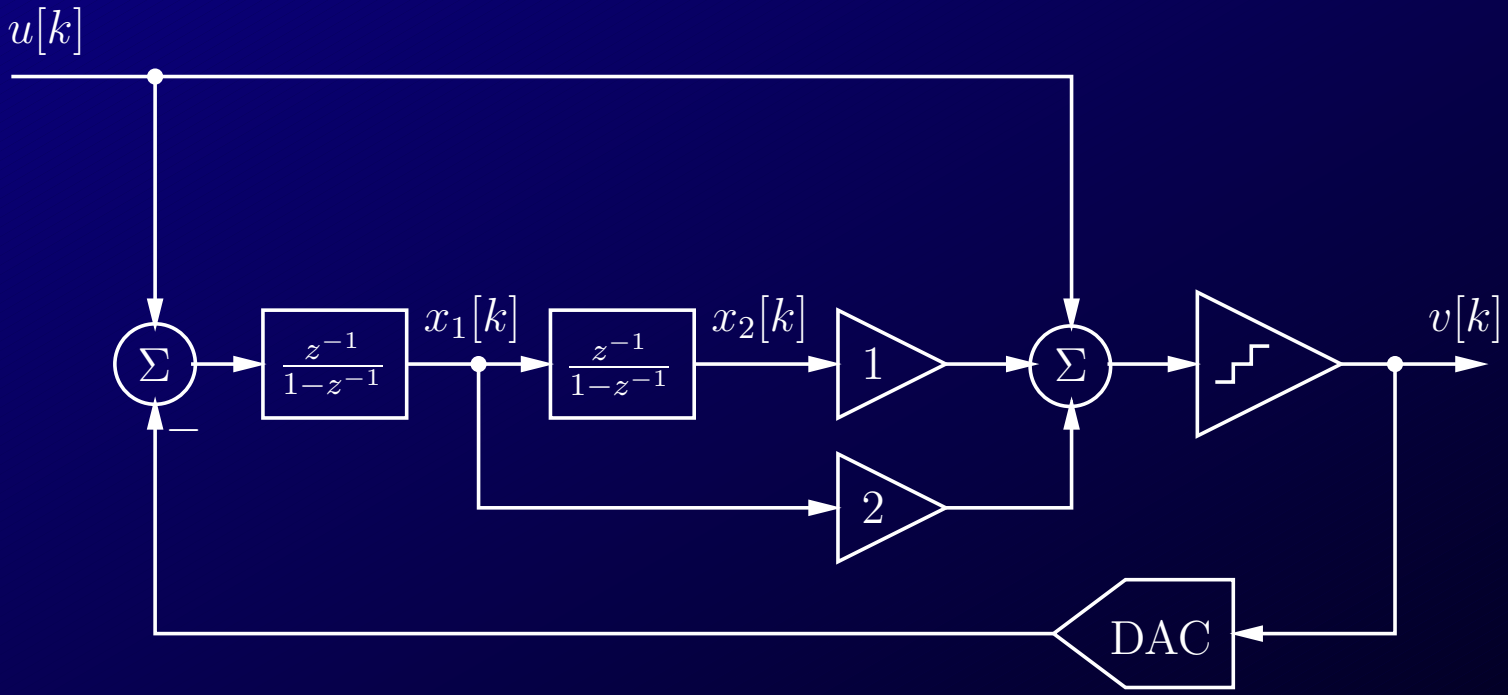
$$= \min_{\alpha} \int_0^{\frac{f_s}{2OSR}} \left(1 - 2(\cos N\alpha) z^{-N} + z^{-2N}\right)^2 df$$

we get

$$\alpha_{\mathrm{opt}} = \frac{1}{N} \cos^{-1} \left(\frac{\sin\left(\frac{\pi N}{OSR}\right)}{\frac{\pi N}{OSR}} \right) = 0.44|_{N=2, OSR=4} \, .$$

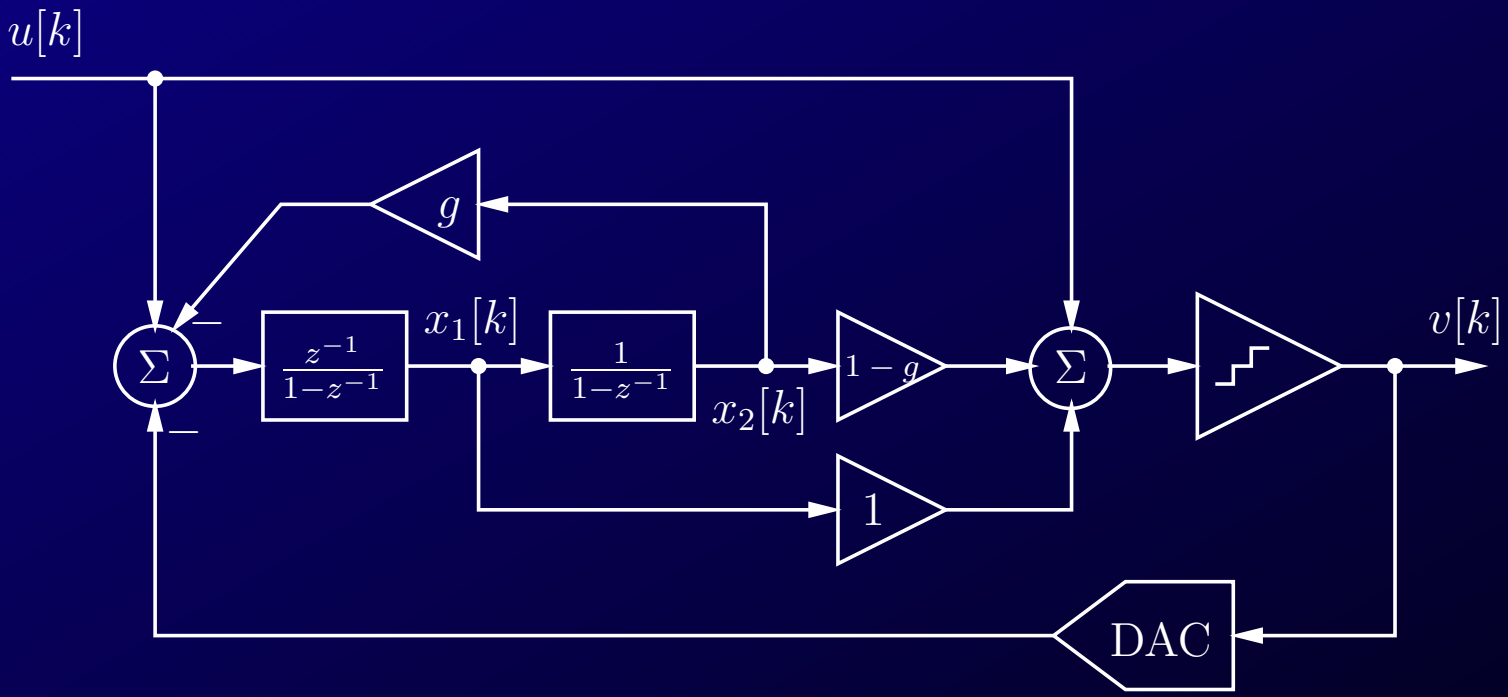
Modifying the NTF:

Original First Stage [Silva01]



$$NTF = 1 - 2z^{-1} + z^{-2}$$

Modifying the NTF:
Modified First Stage

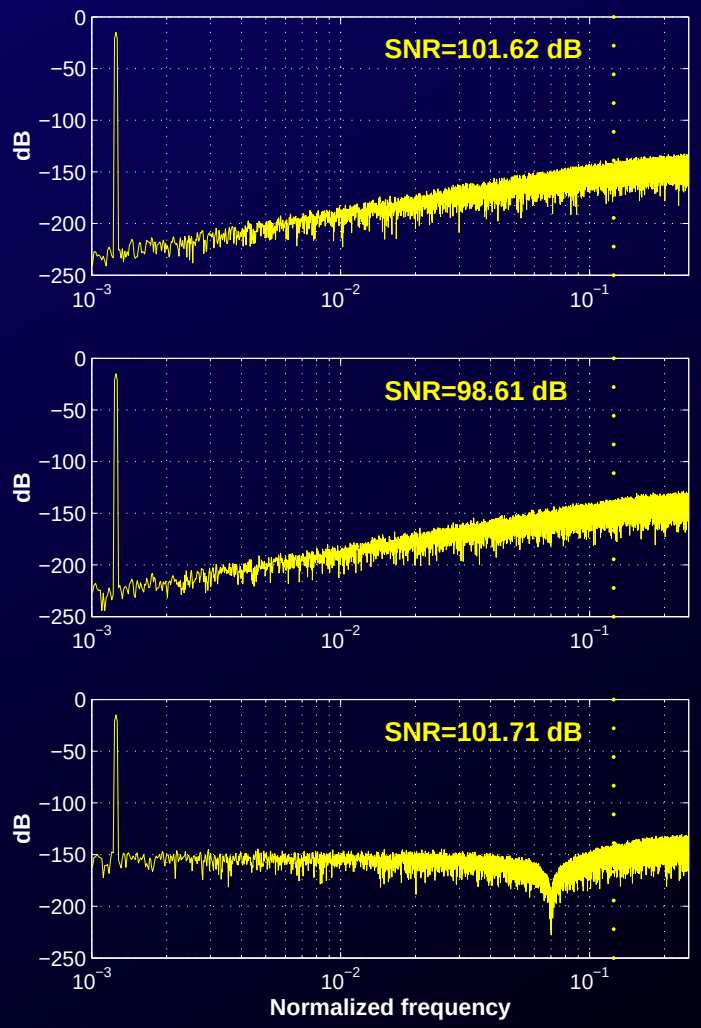


$$NTF = 1 + (-2 + g)z^{-1} + z^{-2}$$

$$g = 2 - 2\cos\alpha = 0.19|_{N=2,OSR=4}$$

Simulation Results

- Full-speed structure w/ 3rd order decimation, SNR=101.62 dB
- Reduced-sample-rate structure w/ 2nd order decimation, SNR=98.61 dB
- Proposed structure w/ 2nd order decimation, SNR=101.71 dB



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